SESSION VI

Processing II – Gate Recessing

Chair: Paul Becker, Sanders, A Lockheed Martin Company

Controlling circuit current (Idss) through gate current prior to metallization is paramount to the yield and performance of MMIC product production lines. This parameter affects breakdown voltage, lifetime, power output and noise figure of production product. Many different processes have been investigated and proposed in production to uniformly and reproducibly control the circuit current. Four papers will be presented in this session that detail different approaches.

One approach in production for 10 years is illustrated in an invited paper from Siemens Semiconductor Group: "Dual Implant One Metal". This method of processing eliminates the need for labor intensive etching of product controlling current through ion implant. Data and results gathered in a decade of production will be reviewed in this paper. Another approach widely utilized in manufacturing is etching of the wafers after gate lithography prior to metallization. This method will be presented in three papers with information regarding MESFET and PHEMT products disseminated. "MESFET Recess Geometry Impact on Idss" presented by TriQuint, and "Development of a Robust Recess Etching Process for MESFET Devices" presented by Watkins Johnson Company, both speak to MESFET ion implant processes utilizing wet recess etching. Information regarding using etch to control current, depth, and sidewall geometry will be presented. The paper "A Double Selective Double Recess Process for Power PHEMT Devices" from Sanders, A Lockheed Martin Company, will describe a selective wet etch process utilized to reproducibly control recess width and current in PHEMT products.

A great deal of data will be presented from an international field of authors in this session. The papers presented will be detailing drastically different approaches. Please plan on attending and participating in this Manufacturing Process Technology Session.