Process Monitoring for Nitride Dielectric Defect Density

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ABSTRACT

We have implemented a process monitor for defects in the silicon nitride deposition sub-process of a GaAs PHEMT fab line. The nitride is used as the dielectric in MIMCAPs (metal-insulator-metal capacitors). The defect monitor is based upon ramped breakdown testing of test capacitors on each wafer. In order to interpret the ramped breakdown data, the TDDB theory was utilized, suitably modified for the silicon nitride dielectric. Six months of process monitoring was carried out and an upper control limit established for the nitride defect density.

INTRODUCTION

The purpose of this paper is to describe the establishment of capacitor defect monitoring in a GaAs PHEMT process. The process, described elsewhere [1] is a 0.15 µm robust low noise, high reliability MBE based process with MIMCAPs (metal-insulator-metal capacitors) and other passive on-chip components. The MIMCAPs utilize PECVD (plasma-enhanced chemical vapor deposited) silicon nitride in two separate layers. The dielectric films are nearly perfect, however there are always inevitable defects and imperfections. This paper shows how it is possible to monitor the nitride quality on a regular basis. An effective process monitor is a requirement for any possible future process improvements.

MIMCAP FABRICATION PROCESS

Fig. 1 shows a cross section of a typical MIMCAP fabricated in this process. The first layer of nitride (nitride 1) is deposited at 250°C atop the GaAs substrate. First interconnect (FIC) metal forms the bottom plate of the MIMCAP. FIC consists of the following e-beam evaporated metals: a thin Ti layer to promote adhesion to nitride 1, a Pt barrier layer, a thick Au layer and a thin Ti layer for adhesion of the capacitor nitride 2. The nitride 2 layer is again formed by PECVD at 250 °C, and has a nominal thickness of 500 Å. Nitride 2 also provides passivation for the PHEMTs. Nitride 3 is deposited at 90 °C and is patterned using a liftoff process so that it is present only in the MIMCAPs. The top metal structure above the nitride 3 layer is formed by sputter deposition of a thin Ti layer followed by a thin seeding layer of Au. Next, Au is electroplated to a thickness of 3.5 µm. The top metal is applied over patterned photoresist which defines the placement of air bridges for connection to adjacent circuit elements. The edges of the top metal as shown in Fig. 1 are set back from the edge of FIC metal as a result of this photoresist mask. The actual test structures used for defect monitoring also include bondpads consisting of stacking both FIC metal and top metal. The capacitor bottom plate is connected to a bondpad using FIC metal. The capacitor top plate is connected to a bondpad (or to other circuit elements in the case of a MMIC) using an air bridge, avoiding corner electric fields at the edge of nitride 3.

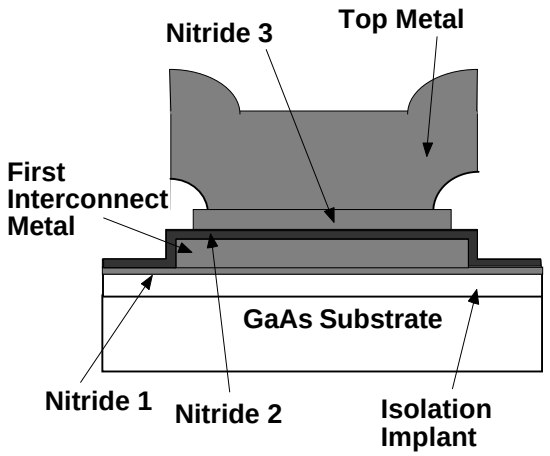

Fig. 1. Cross section of a MIMCAP.

TDDB THEORY

We have adapted the TDDB (time dependent dielectric breakdown) theory originally formulated for the monitoring of defects in silicon MOS technologies [2,3]. However, several modifications to this theory are required. The first is that the dielectric films used in GaAs technologies are silicon nitride rather than silicon dioxide. Silicon nitride is PECVD deposited at a relatively low temperatures of 90 °C and 250 °C (as compared to CVD nitride deposited at 700 °C). The resulting films conduct much more current than in films for silicon-based technologies.

The conduction mechanism in the MIMCAP dielectric is predominantly by Frenkel-Poole conduction [4] given by

$$J_{FP} = \sigma_{FP} E \exp\left[\frac{-\left(\phi_t - \beta\sqrt{E}\right)}{kT}\right] \qquad (1)$$

where ϕ_t is the trap energy level (0.85 eV), σ_{FP} is the Frenkel-Poole conductivity coefficient (2.4×10^{-3} S/cm),

$\beta = \sqrt{\frac{q}{\pi\varepsilon_0\kappa}}$ is the Frenkel-Poole emission coefficient (2.771×10^{-4} $cm^{1/2}V^{1/2}$), ε_0 is the permittivity of free space, and κ is the relative dielectric constant of Si_3N_4, assumed to be 7.5 here. At low electric fields, there is also an Ohmic conduction mode, however it can be neglected since it is the high field conduction at defects which determines the reliability of the MIMCAPs.

A second major difference from silicon-based capacitors is that the dielectrics are relatively thick, and breakdown occurs at relatively high voltages. The dominant failure mechanism of the MIMCAPs is not dielectric wearout, but rather breakdown at defects. The defects in the nitride films control the reliability of the MIMCAPs.

The defects are modeled as sites where the nitride is thinner than the nominal dielectric. These weak spots are very small in area (less than 1 μm^2) and are undetectable in normal operation. While the nominal dielectric has a nitride thickness of d_0, the defects have "effective " thicknesses d_{eff} ranging from 0 up to d_0. It is the distribution of these defects which determines the reliability of the MIMCAPs. There is a statistical distribution of the d_{eff} values themselves, and a probabilistic occurrence of the defects spatially across the MIMCAPs.

Breakdown occurs at the weakest site with the smallest value of d_{eff} in a given MIMCAP. Breakdown is the result of charge accumulation in the dielectric causing the internal field to build up. When a critical charge Q_{crit} is achieved after passage of current density J for a sufficient time, breakdown occurs. The charge to breakdown is defined as $Q_{BD} = Jt_{BD}$ where t_{BD} is the time to breakdown. The critical charge per unit area stored internally that triggers the breakdown is given by

$$Q_{crit} = \eta Q_{BD} = \eta J t_{BD} \tag{2}$$

where η is the trapping fraction, a dimensionless quantity describing the ratio of the charge trapped to the total charge passed through the dielectric. For the two layer dielectric described here, Q_{BD} is approximately 150 Coul/cm^2, and the trapping fraction is about 5 X 10^{-7}.

Combining eqs. (1) and (2), assuming a constant applied voltage, allows the capacitor lifetime to be written as

$$t_{BD} = \frac{Q_{crit}}{\eta\sigma_{FP}\exp\left(\frac{-\left(\phi_t - \beta\sqrt{V/d_{eff}}\right)}{kT}\right)} \tag{3}$$

The capacitor lifetime is dependent upon the applied voltage, the temperature, and the effective nitride thickness d_{eff}. Using this equation, it is possible to determine the minimum allowable effective nitride thickness d_{MIN} to assure a lifetime of 10 years versus temperature for an assumed applied voltage of 5V. This is shown in Fig. 2, where it is seen that for temperatures to 100 °C, the effective thickness must exceed about 750 Å for a 10 year life.

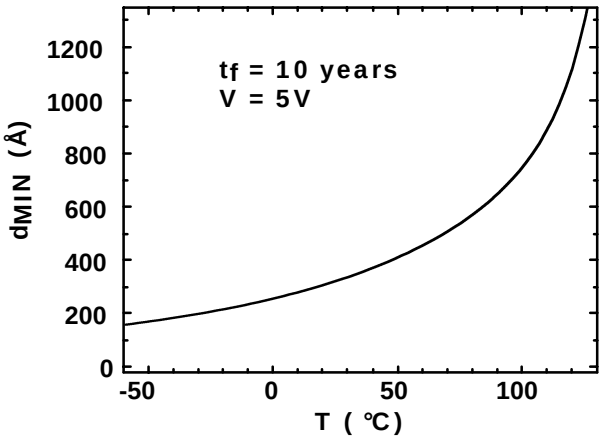

Fig. 2. Minimum effective thickness vs. temperature for a 10 year capacitor lifetime.

Eq. (3) may be generalized to arbitrary voltage and temperature histories. The condition for breakdown can be described as [4]

$$1 = \int_0^{t_{BD}} dt \frac{\eta}{Q_{crit}} \frac{V}{d_{eff}} \times \left[\sigma_{FP}\exp\left(\frac{-\left(\phi_t - \beta\sqrt{V/d_{eff}}\right)}{kT}\right)\right] \tag{4}$$

This expression is useful for predicting the lifetime t_{BD} for a known value of d_{eff} for time-varying applied voltage and temperature. Conversely, if the applied voltage and temperature needed to achieve breakdown in time t_{BD} are known, this information can be used to extract the value of the effective nitride thickness. When the applied voltage is a linear ramp function, the relationship between the ramp breakdown voltage and the effective nitride thickness d_{eff} is nearly linear, as shown in Fig. 3, and can be conveniently described by a quadratic of the form

$$d_{eff} = a_1 V_{BD} + a_2 V_{BD}^2 \tag{5}$$

where a_1 and a_2 are constants given by 16.8 Å/V and 0.0122 $Å^2/V^2$ respectively.

RAMPED BREAKDOWN METHOD

We have implemented the ramped breakdown technique based upon eq. (4) as a process monitor for the nitride defect density in our 0.15 µm PHEMT process. Test capacitors of area 12,040 μm^2 are used. On each wafer, 22 of these capacitors are tested. A ramp rate of 25 V/sec is supplied using an HP 4142B analyzer with a pair of HP 41421B plug-ins. The plug-ins are arranged so that the top metal plate of the capacitor is swept positively, while the bottom plate (FIC metal) is simultaneously swept negatively for a maximum possible voltage of 200V across the capacitor. Since the current compliance of these plug ins is limited to 20 mA, breakdown is defined at the voltage at which this 20 mA compliance is achieved. With a ramp rate of 25V/sec, the ramped breakdown test requires 8 seconds per capacitor tested.

Fig. 4 shows a group of superimposed IV characteristics obtained during the ramped voltage test of approximately 100 capacitors. As can be seen, all the capacitors exhibit an abrupt breakdown as the current suddenly rises to the current compliance of the test equipment. In this set of data, most of the capacitors break down at voltages greater than 60 V. One capacitor in this sample had a low breakdown voltage of 6 V. In many cases, the capacitors reach the current compliance of the equipment before reaching a definite breakdown condition.

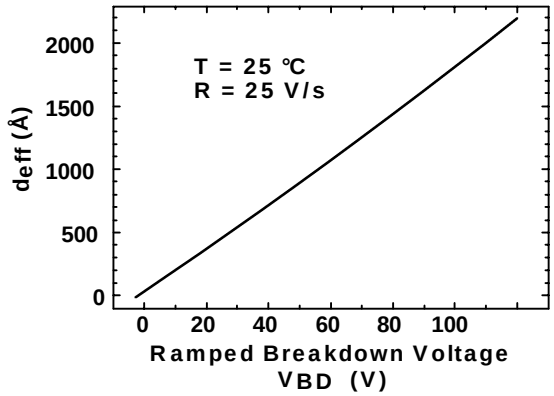

Fig. 3. Transformation from ramped breakdown voltage to nitride effective thickness.

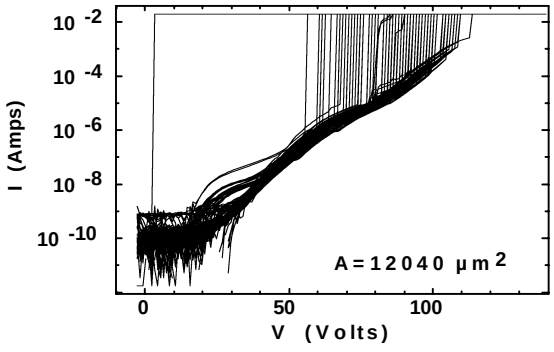

Fig. 4. IV characteristics of approximately 100 test capacitors.

DEFECT MODEL

Fig. 5 shows a probability plot of approximately 5500 test capacitors from 42 lots (there are six wafers per lot) measured over about a 6 month period. Four distinct regions are evident on this probability plot. The first is labeled "dead on arrival" and represent capacitor shorts. These capacitors are not a reliability concern since they are screened out during RF and electrical testing. However they should be monitored as a potential yield limiting factor. Another category is labeled "current compliance". These capacitors did not break down before the equipment current limit was reached, and are plotted at the 100 V mark. They do not pose a reliability or yield risk. The segment labeled "intrinsic defects" lies above 40 Volts, and represents defects with d_{eff} greater than about 700 Å. From Fig. 2, these are not considered a reliability or yield concern. These defects are a characteristic of the nitride film itself. The region labeled "extrinsic defects" are the yield and reliability limiting defects that should be monitored.

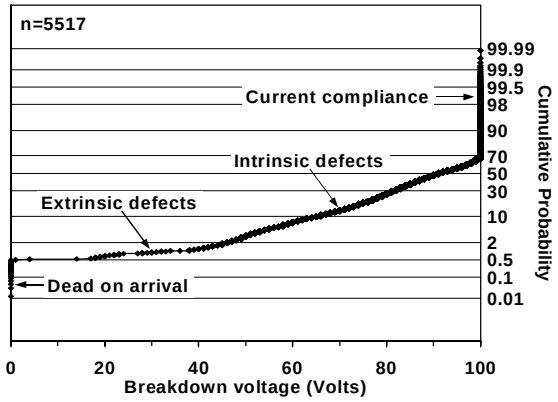

Fig. 5 Probability plot of approximately 5500 capacitors tested over a six month period.

The extrinsic defects are postulated to have many causes, such as MBE defects in the starting wafer, metal defects or "spits" from the FIC metal deposition, inhomogeneities or particles from the nitride PECVD deposition, or particles or residue from the nitride 3 liftoff process.

The defect density can be estimated from the Seeds defect model [5] given by

$$P = DAe^{-DA} \approx \frac{DA}{1+DA} \tag{6}$$

where P is the probability of a defect, D is the defect density and A is the area of one test capacitor. Using this model, the defect density can be computed as

$$D \approx \frac{1}{A}\left(\frac{P}{1-P}\right) \tag{7}$$

DEFECT MONITOR

It is desirable to have a weekly monitor of the defect densities. Each week, the probability of dead on arrival defects is calculated as N_d/N, where N_d is the number of dead on arrival defects (defined as $V_{BD} \leq 5V$) per week, and N is the total number of capacitors tested in that week. The defect density is then calculated directly using eq. (7). The probability of extrinsic defects is similarly calculated as N_e/N where N_e is the number of extrinsic defects (defined as $5 < V_{BD} \leq 40$) per week. The lower (light) lines in the control charts of Figs. 6 and 7 show the data calculated in this fashion.

Note that in some weeks there will inevitably be zero capacitor defects, either because the defect density is low for that week, or because insufficient quantities of capacitors happened to be available for testing in that week. A more realistic upper bound on the defect densities under these circumstances is found from substituting upper probability bounds $(N_d + 1)/(N + 1)$ for dead on arrival defects, and $(N_e + 1)/N + 1)$ for extrinsic defects. The upper bounds are plotted in Figs. 6 and 7 as the upper (heavy) lines. They are always non-zero.

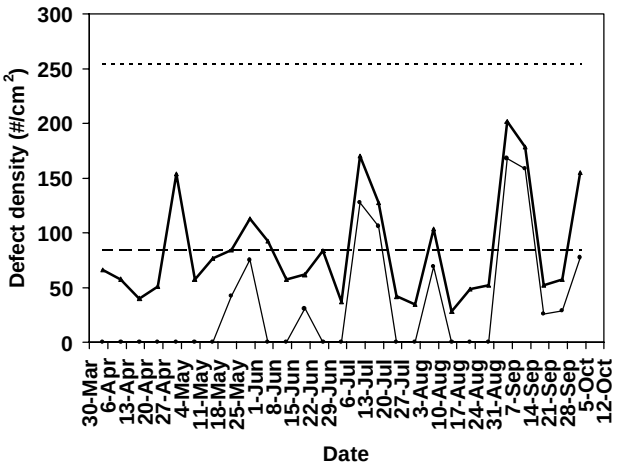

Fig. 6 Dead-on-arrival defect density control chart

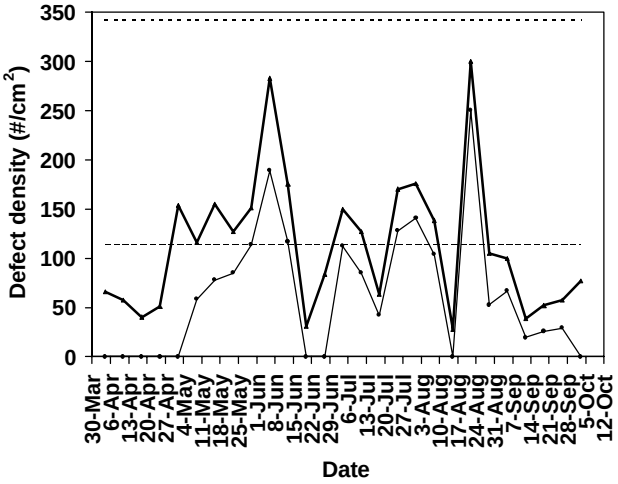

Fig. 7 Extrinsic defect density control chart.

The defect densities are quite variable from week to week, similar to results seen in silicon MOS technologies. The defect densities tend to follow a Poisson distribution in time, with the probability of zero defects in a capacitor with area A given by e^{-DA}. The probability of one defect in area A is given by DAe^{-DA} (identical to the equality in eq. 6). It is not possible using ramped tests to determine if there are any more than one defect per capacitor since the weakest defect always breaks down first.

The six-month mean defect densities are shown by the lower dashed lines in Figs. 6 and 7. Upper control limits established at the "+3-sigma" level are simply three times these mean values since the standard deviation for a Poisson process is equal to the mean. The recommended upper control limits are the upper dashed lines in Figs. 6 and 7.

SUMMARY

We have described an in-process monitor for silicon nitride dielectric used for MIMCAPs in an PHEMT process. The monitor is based upon performing ramped breakdown voltage sweeps of test capacitors on every wafer. An upper bound on the defect density was computed from the statistics on a weekly basis. Two types of defects were considered — those that affect yield, and those that affect reliability. Over six months of data show the process capability for both types of defects, and upper control limits were established. Based upon these results, it is planned to perform nitride defect monitoring across all other TRW fabrication processes.

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