# InP HBT Production Technology for 100 Gbps Lightwave Communications

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ABSTRACT

**InP HBT technology appears to offer the high speed, low power and basic producibility necessary to support a high-speed digital IC technology. Maximum clock speed of 53 GHz has been demonstrated at 40 mW per flip-flop (FF) as compared to well over 200 mW/FF for SiGe at slower speeds. At a power dissipation of less than 9 mW/FF, toggle rate is still a respectable 35 GHz. Producibility and high speed at reasonable power levels are what set InP HBT apart from other high-performance technologies. For reasonable levels of total power dissipation on-chip, InP actually supports the highest levels of integration of ultra-high speed components: 250 equivalent gates for 5W power dissipation at 50 GHz. In this paper, speed and power of InP HBT are compared to other digital IC technology options such as SiGe HBT and GaAs/AlGaAs HBT, it is shown that InP HBT are ideal for MSI level communications circuits such as multiplexers and demultiplexers. Producibility issues and process latitude are discussed in detail. Yields of circuits demonstrated in this work indicate that levels of integration consistent with 500-1000 transistors are currently realizable.**

INTRODUCTION

In both wireline and wireless communications systems there is an increasing need for circuitry capable of 40, 80 or 100 Gbps data rates[1]. Once received, signals can be demultiplexed and processed at much lower data rates so the primary need is for small and medium scale integrated circuits such as drivers, multiplexers and demultiplexers. Other applications such as $\Delta\Sigma$ data converters also require modest complexity and extremely high clock rates to achieve the desired oversampling ratios. Access to an ultra-high speed, MSI-LSI complexity technology is thus an essential capability for the system engineer. InP HBTs provide the necessary level of complexity and speed for these important applications.

We have previously demonstrated a static divider operating at 52.9 GHz maximum toggle rate[2]. This level of performance enables MUX and DMUX circuits operating at 100+ Gbps[3],[4]. The divider circuit is of sufficient complexity both in transistor count and feedback scheme (in this case: 85 transistors, 36 resistors) to test such issues as device uniformity, device and interconnect parasitics and passive component targetability. Poisson statistics can be effectively used to project yields of more complex circuits from divider yield.

In this paper we report on some of the tradeoffs affecting producibility and manufacturability. In many cases we have opted for highly robust processes instead of those that produce spectacular device results. Optimum circuit performance was obtained with the relatively modest device unity current gain cutoff frequency, $f_t$, of 135 GHz and a corresponding maximum frequency of oscillation, $f_{max}$, of 240 GHz. Unlike the deep submicron gates required by advanced HEMT processes[5], the InP HBT transistor layout uses conventional optical lithography with 1μm minimum feature size throughout. Base doping is maintained at a level previously demonstrated to be reliable[6]. Robustness of the technology is further demonstrated by the fact that a range of epitaxial structures produced essentially equivalent circuit performance. This work demonstrates that InP based HBT circuits are producible with clock rates well in excess of 40 GHz and that the technology is sufficiently mature *now* to yield 500-1000 transistor circuits.

TRENDS IN HIGH SPEED CIRCUITS

Divider frequency has increased from 4 GHz to 53 GHz in the approximately two decades since the first demonstration of a III-V (GaAs) based static divider[7]. Figure 1 shows that the trend has not been a smooth one for III-V based technology but has been fairly predictable for Si based technology. The period of rapid advance in the mid to late 1980's roughly corresponds to the U.S. defense buildup while the lull in the early 1990's corresponds to the DoD procurement downturn. The smooth Si trend is likely to be more a function of demand in commercial and industrial markets than to the whims of the defense market. The recent resurgence in the rate of increase of III-V speed, however, seems to be more driven by the globally expanding communications market than by defense expenditures… an encouraging trend for III-V.

At the current rate of increase, maximum clock rates will exceed 100 GHz sometime in the next two years and they will approach 1 THz in the next decade. A number of issues need to be addressed to achieve producible technologies at these clock rates. Of course the underlying device technology must have sufficient cutoff frequency but cutoff frequencies (both $f_t$ and $f_{max}$) of roughly twice the clock rate should do. Equally important are compactness of design, a low permittivity dielectric and signal line shielding. Taken together these three requirements can best be achieved with a multiple level

interconnect (at least 3 layers) and a readily planarized dielectric such as polyimide or BCB. In addition, device matching must be maintained as devices are scaled and clock speeds increase. Well matched devices allow the differential logic gates to operate with small signal swings.
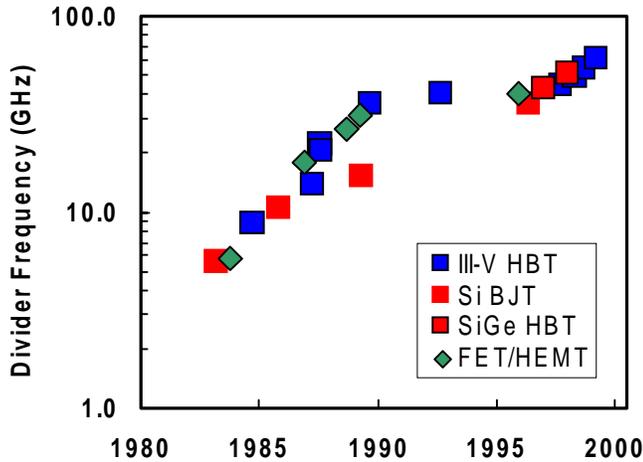


Fig. 1 – Historical trend in maximum clock-rate of static dividers. Points include published accounts that claim the highest overall circuit speed or highest speed in one of the listed technologies.

PRODUCIBILITY

The device structures for this work were grown by solid source molecular beam epitaxy (MBE) as described previously[8]. Frequency dividers and ring oscillators were fabricated in a reduced parasitic, 4 μm wire-pitch AlInAs/InGaAs HBT IC process. The process includes a self-aligned base metal to the emitter but optically aligned collector and base contacts. Contact to the device is made with second level metal. The interlayer dielectric is polyimide, planarized in an Inductively Coupled Plasma (ICP) etcher which is also used to define the via contacts[9]. A focused ion beam cross-section of a 1μm device is shown in Fig. 1. The micrograph shows the nearly planar surface above the HBT which is essential for multi-level interconnect.
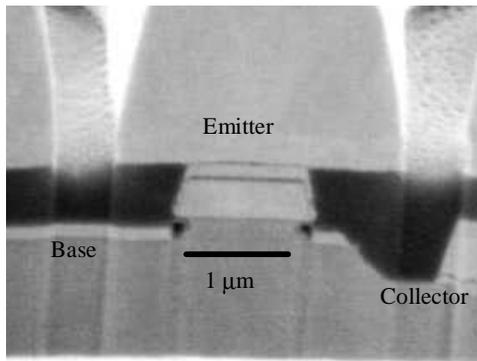


Fig. 2 – Focused Ion Beam cross-section of 1μm AlInAs/GaInAs HBT.

A key advantage of bipolar transistors (both HBT and BJT) is that the physics of the base-emitter pn junction determines the turn-on voltage. In field-effect devices: MESFETs, HEMTs and MOSFETs, the specifics of doping, implant depth or oxide thickness determine the threshold voltage. Thus, in general and especially in III-V compound semiconductors, the turn-on uniformity for bipolar transistors is superior to that for field effect devices. This is true of both long range (wafer) uniformity and short range (pair match) uniformity. A typical result of pair match uniformity for InP HBT is shown in figure 3. Typical field-effect technologies report threshold standard deviation of about 10 mV, here the standard deviation of $V_{be}$ turn-on is less than 2 mV. Differential logic gates with closely matched device pairs will operate correctly even at very small input logic swings. This is essential for high frequency operation where signal attenuation, particularly at the input, can be severe.
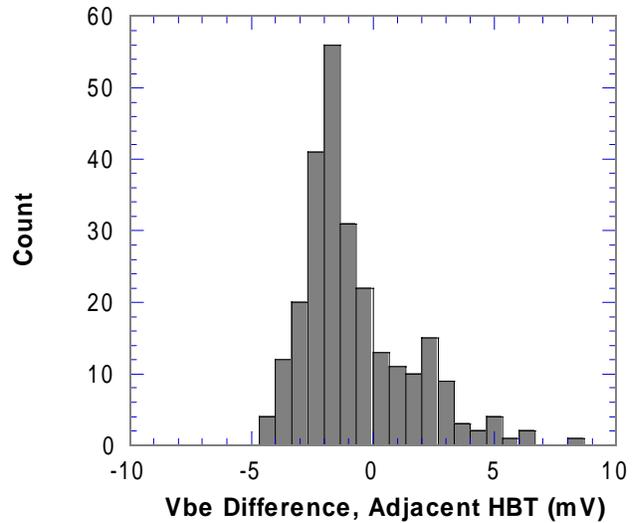


Fig. 3 – Distribution of the difference in measured $V_{be}$ (at high current density) between adjacent (50 μm spaced) 1x3 μm HBT.

There are two common misconceptions driving technology selection for high speed circuits. One is that Si based technology provides higher levels of integration than III-V technology because of its maturity. The second is that bipolar logic is more power hungry than field-effect transistor based logic. While each of these statements is true for many classes of integrated circuits, it is decidedly false for ultra-high speed circuits. At a clock rate of 50 GHz, for reasonable levels of power dissipation on-chip, InP HBT provides significantly more integration capability because of its lower power dissipation per gate than SiGe technology. Figure 4 plots the available gates/watt of power dissipation[10,11,12,13,14]. The maturity of InP processes is sufficient to 250 gates at a 5W on-chip total power dissipation. The integration level is *power* constrained not yield constrained. The figure also plots the best speed/power results for a HEMT-based logic family; the power dissipation per gate is calculated from the total power

of a representative circuit, a 256/258 dual-modulus prescaler[15] not from more idealized ring oscillator data.
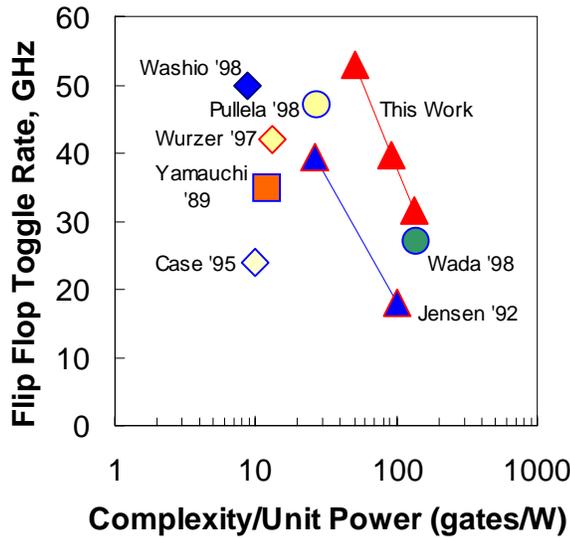


Fig. 4 – Power constrained circuit complexity for a number of high speed technologies reported in the literature.

DEVICE AND CIRCUIT PERFORMANCE

Unity current gain cutoff frequencies as high as 225 GHz were obtained for larger devices (1.5x8μm) and matched $f_t$ and $f_{max}$ were obtained at about 180 GHz for smaller transistors (1x3μm). Devices as small as 0.7x0.7 μm (effective emitter area) have been fabricated operating at $f_t=f_{max}=160$ GHz. Device selection for high speed logic circuits is based on a tradeoff of speed and power dissipation. Larger area transistors have higher cutoff frequency but significantly higher power. Divider circuit designs were based on 1x3μm devices, which offer 93% of the cutoff frequency of long emitter structures. Scaling of $F_t$ and $F_{max}$ with emitter size are plotted in Fig. 5. Typical model parameters for 1, 3 and 5 μm HBT are listed in Table I.

TABLE I
TYPICAL HBT MODEL PARAMETERS

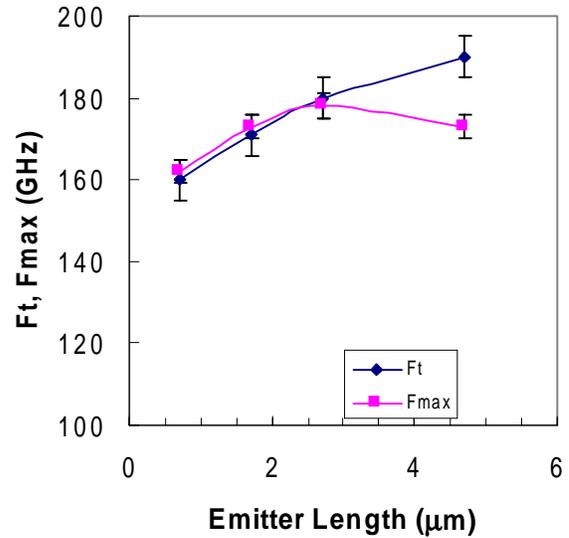| Parameter | Symbol | 1x1 μm | 1x3 | 1x5 |
|---|---|---|---|---|
| Current Gain | $\beta$ | 40 | 40 | 40 |
| CE Breakdown | $BV_{ceo}$ | 2.9 V | 2.9 | 2.9 |
| Base Resistance | $R_B$ | 173 Ω | 67 | 34 |
| Collector Res. | $R_C$ | 13.7 Ω | 10.4 | 10.4 |
| Emitter Res. | $R_E$ | 23.4 Ω | 6.8 | 3.6 |
| CB Capacitance | $C_{JC}$ | 9.3 fF | 13.1 | 17.0 |
| EB Capacitance | $C_{JE}$ | 2.0 fF | 8.7 | 16.5 |



Fig. 5 – Cutoff frequency (ft, fmax) scaling for 1μm emitter stripe-width HBT.

Divider design has been reported previously[16]. A micrograph of the circuit is shown in Fig. 6. The overall chip size is 0.6x1.2 mm; however, excluding pads the circuit area is only 0.1mm². Divider maximum toggle rates for four wafers are shown in figure 7. The maximum clock frequency is very similar for four distinct material structures that represent the process "corners". This is further evidence that divider toggle rate is not limited by the transistors but rather by particular device and circuit parasitics not captured in the cutoff frequency figures of merit.
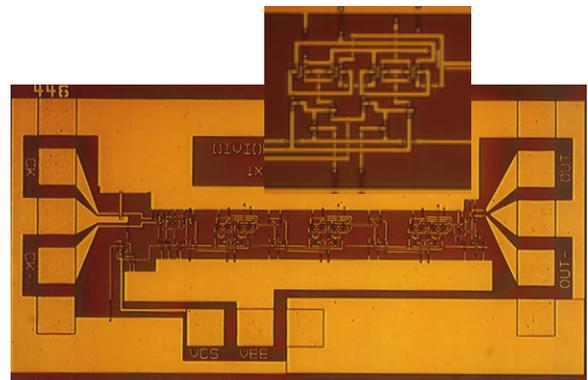


Fig.6 – Photomicrograph of divide by eight circuit with a detail of the flip-flop (inset). The overall circuit dimensions are approximately 0.6 x 1.2 mm.
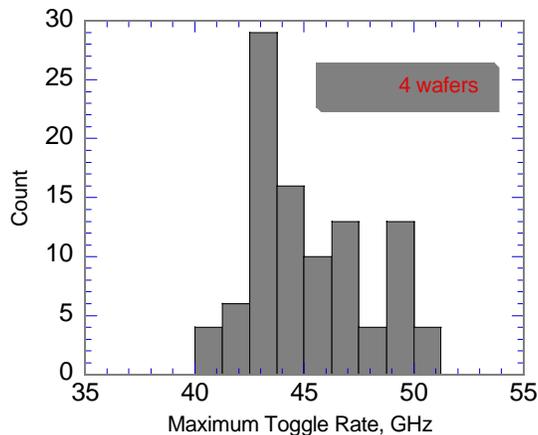
Fig. 7 – Distribution of maximum toggle rates on-wafer at fixed power supply voltage of –3.1V and input signal of 500 mV peak-to-peak.

## DISCUSSION

The essential circuits required for a high data rate transmission system are MUX, DMUX, clock and data buffers, output buffers and output drivers, and clock and data recovery circuits. All of these circuits are relatively simple, requiring small or medium scale integration. Additionally, all of the circuits can be built up from the same building blocks used to realize the static divider in this work. To operate at 100 Gbps, the clock rate must exceed 50 GHz at a minimum. This clock speed requires considerable power dissipation in the circuit regardless of the technology. InP HBT is competitive in all three critical dimensions: speed, power and uniformity required to realize MSI ICs. Other technologies have critical deficiencies: SiGe consumes too much power, E/D HEMT is limited by non-uniformity in threshold voltage, GaAs based HBTs require high power (because of higher turn-on voltage) and do not have the inherent speed required.

## SUMMARY

We have demonstrated InP HBT technology capable of 100 Gbps data rates. Power dissipation, yield and process uniformity are consistent with the ability to produce 4:1 MUX and 1:4 DMUX circuits. Based on speed, power and producibility advantages, InP HBT appears to be the ideal technology for high data rate circuit applications.

## ACKNOWLEDGEMENT

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