0.1 µm InGaAs/InAlAs/InP HEMT Production Process for High Performance and High Volume MMW Applications

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ABSTRACT

We have developed a unique production process based on 75 mm diameter InP substrates and 0.1 µm passivated InP HEMT devices. Our InP HEMT MMIC technology has demonstrated state-of-art low noise performance from 2-200 GHz. We present here over 2000 manufactured 44 GHz LNAs with greater than 80% yield and typical performance of 25 dB gain and 2.2 dB noise figure. We have also compiled statistical process data from approximately 100 recently fabricated 0.1 µm 75 mm InP HEMT MMIC wafers which demonstrates the consistent performance and repeatability of our process over a 6-8 month period.

INTRODUCTION

As the needs for MMW systems spreads from the DoD domain into the commercial world, the drive for higher performance MMICs with simultaneously higher volume capacity have become evident in the past few years. InGaAs/InAlAs/InP HEMTs have demonstrated the highest gain, lowest noise and highest frequency capability for any three terminal transistor [1-4] and are a natural fit towards next generation satellite communication systems, wireless LAN and ultra-high frequency remote sensing applications to name a few. A further advantage, especially for array type of applications is the ultra-low d.c. power dissipation of these transistors.

PROCESS DESCRIPTION, TREND CHARTS

To transition into a viable production process efficiently, TRW has leveraged several aspects of its high volume 0.15 µm InGaAs/AlGaAs/GaAs HEMT (GaAs HEMT) production process[5] into the 0.1 µm InP HEMT process. The two processes share 75% commonality with the only major differentiation occurring with the chemical etchants, annealing conditions and backside processing. The process flow of the 0.1 µm InP HEMT process flow is nearly identical to that of the production 0.15 µm GaAs HEMT process. Furthermore, similar design rules and device topologies are used for both processes, simplifying the design and layout of MMIC circuits. Other key MMIC process parameters include a silicon nitride passivation thickness of 75 nm, silicon nitride MIM capacitors with a 300 pF/mm^2 sheet capacitance and precision NiCr resistors with 100 ohm/sq. sheet resistance[6,7].

The key issues with the development of the InP HEMT process are in MBE growth of high quality HEMT epitaxial material on 75 mm InP substrates, definition of 0.1 µm gates and repeatable gate recess etching and the development of a robust backside dry via etch process. The InP HEMT epitaxial structure shown in Figure 1 has been TRWís baseline structure for low noise amplifiers for several years [1,2,6.7].

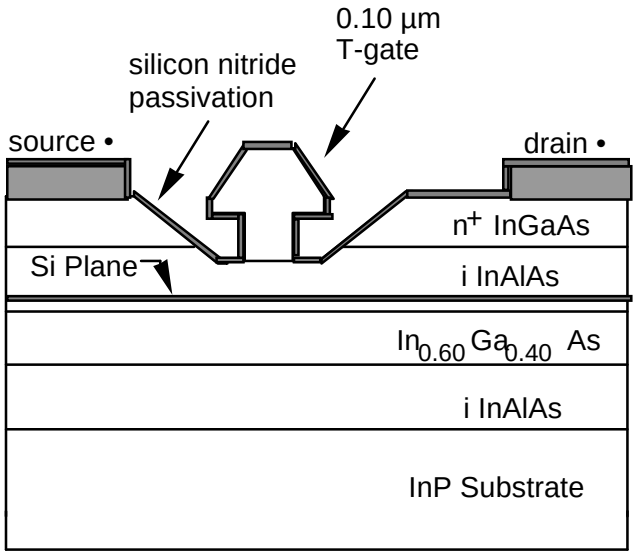

Figure 1. Cross-sectional view of MBE grown InGaAs/ InAlAs/InP HEMT profile

Improved substrate quality combined with optimized growth conditions and techniques have resulted in excellent material quality and repeatability. A target sheet concentration of 3.5 x 10^{12} cm^2 and mobilities in excess of 10,000 cm^2/V-sec are typically achieved for the InP HEMT structure with a 60% indium composition pseudomorphic InGaAs channel.

A key to the reproducibility of the InP HEMT device is the definition of the 0.1 µm (100 nm) T-gate with electron-beam lithography. Figure 2 shows the trend chart of the measured gate length based on two end-view SEM measurements of gate fingers taken for each wafer fabricated. An average end measured gate length of 90 nm with a standard deviation of 9 nm or 10% has been achieved. Correlation with cross-sectioned gate shows that the end-view measurement is approximately 1 nm or 0.01 µm smaller than the cross-sectioned gate length.

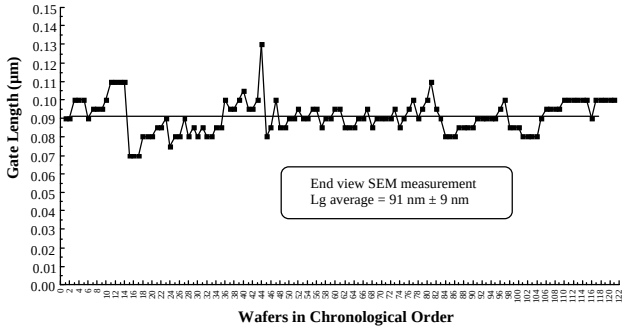

Figure 2. Gate Length trend chart for 0.1 µm InP HEMT MMIC process

Figure 3 shows the high device yield attained wafer to wafer on this process, with most wafers attaining better than 90% yield after completion of front-side processing. Even more crucial is the lateral and vertical control of the gate recess, which have significant implications on pinchoff voltage, transconductance and breakdown. The baseline process presented here is a non-selective phosphoric-based recess etchant and has been tailored to achieve repeatable control of the recess profile. Further improvements are expected as selective etchants are introduced into the process.

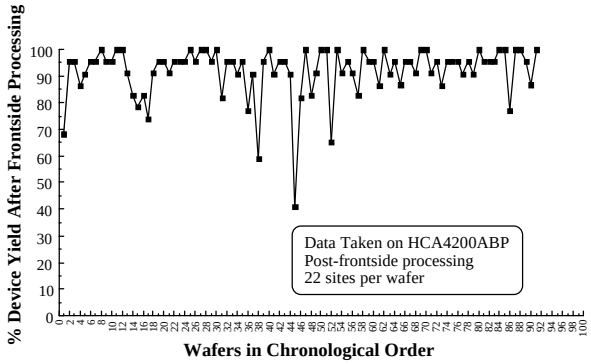

Figure 3. Device yield trend chart for 0.1 µm InP HEMT MMIC process (post-frontside processing)

Trend charts for the voltage at peak transconductance (Vgp) and peak transconductance (Gmp) are shown in Figures 4 and 5 and demonstrate both the high performance and good repeatability wafer to wafer. For 0.1 µm pseudomorphic 60% InGaAs channel devices, we typically achieve a peak transconductance (Gmp) of 900-1000 mS/mm with a cutoff frequency (fT) of 180-200 GHz at 1V drain bias. For each wafer, d.c. characteristics are measured on up to 25 test devices (4 finger, 200 µm total gate width). The wafer average Gmp at 1V drain bias exhibits 920 mS/mm average with a standard

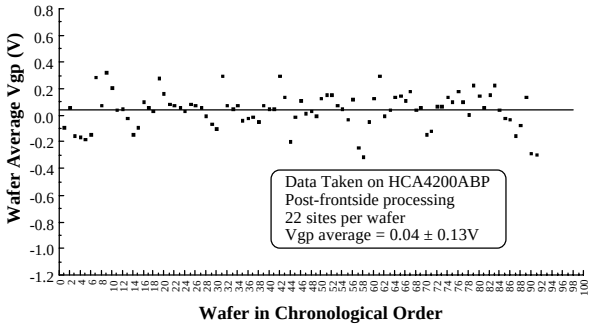

Figure 4. Wafer average Vgp (Peak Transconductance Voltage) trend chart for 0.1 µm InP HEMT MMIC process

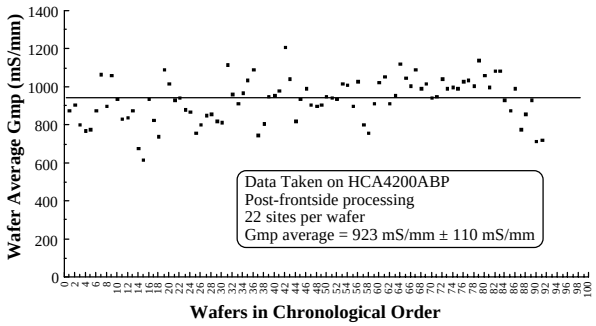

Figure 5. Wafer average Gmp (Peak Transconductance) trend chart for 0.1 µm InP HEMT MMIC process

deviation of 110 mS/mm. Wafer average Vgp (gate voltage at peak Gm) at 1V drain bias was +0.04V average with a standard deviation of 0.13V.

We have recently implemented a robust InP backside process with a dry etch via. Dry etch vias not only enhances device and MMIC performance [9], but is critical to achieve the yield and backside process repeatability necessary for a production process. After lapping and polishing the wafers to 75 µm thickness, through substrate vias were dry etched with a photoresist mask in HBr and BCl_3 gases at a baseplate temperature of 150•C. The plasma conditions were optimized to achieve a high etch rate with good etch selectivity of InP and a high aspect ratio. The via etch pattern was a 40 µm diameter circle and the resultant etched via is a 50 µm circle at the top of the wafer (frontside pad is 120 µm diameter) and less than 80 µm diameter circle at the bottom of the wafer. After via etch, the wafers were sputtered and plated with Ti/Au up to 3.5 µm total metal thickness. The wafers were demounted and flipped for on-wafer circuit test. Visual inspection of etched vias showed excellent yield and after demount, the wafers suffered no visible mechanical damage to airbridges and device fingers.

InP HEMT MMIC Performance and Yield

TRW has demonstrated a family of state-of-the-art MMW LNAs ranging in frequency from 2 GHz to 200 GHz with the 0.1 µm InP HEMT MMIC technology on 50 mm and 75 mm diameter substrates over the past few years[6-8, 10-13].

Freq. (GHz)	LNA Description	Noise Figure	Gain
9-16*	1-stage balanced LNA	1.4 dB	12 dB
20-22*	2-stage single ended LNA	1.0 dB	17 dB
33-37	2-stage balanced LNA	1.7 dB	18 dB
42-47	2-stage single ended LNA	1.7 dB	22 dB
56-64	3-stage single ended LNA	2.0 dB	20 dB
92-96	3-stage single ended LNA	2.9 dB	18 dB
85-95	2-stage LNA (cooled to 6K)	0.7 dB	12 dB
95-105*	4-stage LNA (cooled by 6K)	0.5 dB	20 dB
112-120*	3-stage single ended LNA	3.9 dB	18 dB
139-142	2-stage single ended LNA	5.8 dB	9 dB
150-157	3-stage single ended LNA	5.1 dB	10 dB
165-190	2-stage balanced LNA		7.2 dB

Figure 6. TRW's state-of-art InP HEMT MMIC LNAs (*indicates results have not been published)

We have established several of these data points on the same wafers shown in the trend charts (Figures 2-5). For example, a state-of-art 3-stage single ended low noise amplifier with 4.0 dB noise figure and 17 dB gain at 112-120 GHz [11] and 3-stage single-ended low noise amplifier with 3.3 dB noise figure and 18 dB gain at 94 GHz were demonstrated [6]. We have also recently demonstrated the first 190 GHz low noise amplifier with an enhanced but similar InP HEMT MMIC process on 75 mm InP substrates[8].

A good example of the manufactuability of our process was shown in a recent demonstration. In this demonstration, we demonstrate not only state-of-art Q-band noise figure performance, but excellent wafer to wafer yield and circuit yield. 17 InP HEMT MMIC wafers were completed over 3 wafer lots and they were part of the ~100 wafers shown in the trend charts (Figures 2-5). These wafers were also processed with the dry etch backside vias described in the previous section. More than 2000 circuits were measured over the 17 wafers and the cumulative histogram is shown in Figure 7 with a median performance of 25 dB gain and 2.0-2.2 dB noise figure at 44 GHz.

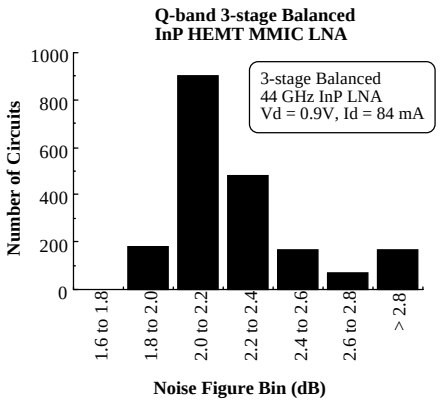

Figure 7. Noise figure histogram of over 2000 tested Q-band 3-stage MMIC LNAs

High MMIC circuit yields for each wafer of approximately 80% have been achieved as shown in Figure 8. The higher yield is partly attributable to the new dry etch via process as we achieved higher yield compared to previous wafers processed with wet etched backside vias.

Not only were high yield and repeatability demonstrated on these wafers, the amplifiers demonstrate state-of-art low noise_performance over the measured 42-47 GHz as shown

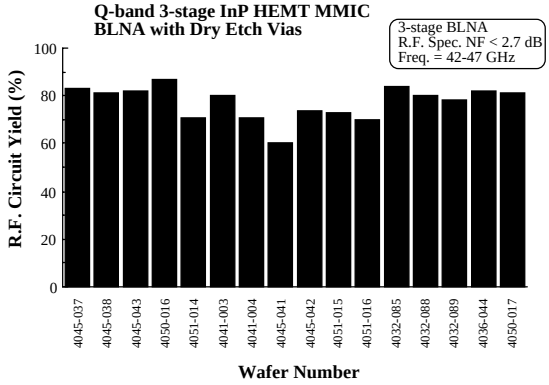

Figure 8. Wafer to wafer r.f. circuit yield for 3-stage InP HEMT MMIC LNA to noise figure specification less than 2.7 dB from 42-47 GHz

in Figure 9 with less than 2.2 dB noise figure across the entire bandwidth (based on wider bandwidth measurements on sample parts, the frequency response for these chip is 36-48 GHz).

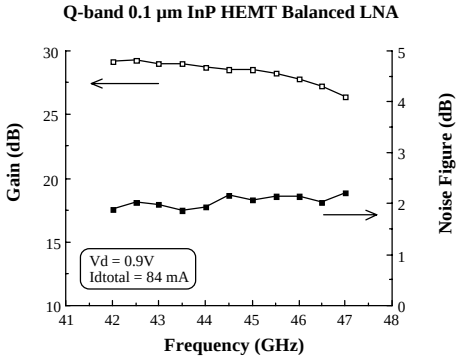

Figure 9. Frequency response of 3-stage Q-band InP HEMT MMIC LNA

CONCLUSION

In conclusion, we have described our development and establishment of a production worthy 0.1 µm InP HEMT MMIC process on 75 mm InP
substrates. The process has demonstrated consistent wafer to wafer performance and statistical control as well as outstanding state-of-art MMW LNA performance. As an example, Q-band MMIC LNAs fabricated using this process has achieved very high RF circuit yield of 80% on over 2000 tested circuits and over 17 fabricated wafers. We feel further enhancements in yield and manufactuability will be achieved in the future with improvements in gate recess etching, and backside processing.

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