$In_{0.5}Ga_{0.5}P$ Etch-Stop Process for PHEMT Manufacturing

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Abstract

A selective gate recess process for Pseudomorphic HEMTs utilizing $In_{0.5}Ga_{0.5}P$ as the etch-stop layer has been developed. This process employs conventional sulfuric acid etch chemistry to obtain 150:1 GaAs/$In_{0.5}Ga_{0.5}P$ etch selectivity. Due to its small conduction band offset, inclusion of the $In_{0.5}Ga_{0.5}P$ layer in the epitaxial structure does not increase the ohmic contact or FET source resistances. PHEMTs fabricated with $In_{0.5}Ga_{0.5}P$ etch-stop layers show no degradation in critical DC and RF parameters when compared to similar non etch-stop devices.

Introduction

Pseudomorphic High Electron Mobility Transistors have gained wide acceptance as the device of choice for a broad range of applications. The extensive use of PHEMTs in both commercial and military systems stems form their significant performance advantage in comparison to GaAs MESFETs. However, this performance advantage comes at the price of a more challenging process, particularly in the critical gate recess operation. Due to the unique carrier profile of the PHEMT, the effective doping level under the gate is over $10^{18}cm^{-2}$. This high doping level results in a rapid rate of current change during the gate-recess operation as the target value is approached (figure 1), a discussion of which can be found in reference [1]. The effect of this etch depth/drain current characteristic is less precise control over PHEMT I_{dss} and V_p as well as a degradation in the uniformity of current dependant device parameters. The critical gate-recess operation is greatly simplified by the incorporation of an etch-stop layer within the PHEMT epitaxial structure. With the inclusion of an etch-stop layer, the target values and uniformity of critical FET parameters (Idss, gm, Imax, Vp, etc.) are solely determined by the epitaxial growth process.

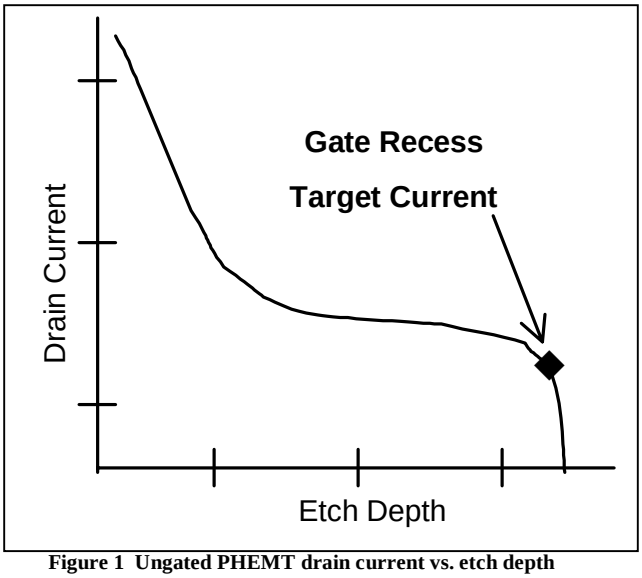

Figure 1 Ungated PHEMT drain current vs. etch depth characteristic

Considerable work has been performed by a number of groups to develop a gate recess etch-stop process suitable for GaAs MESFETs and PHEMTs [3,4,5]. The most common approaches utilize a thin $Al_xGa_{1-x}As$ layer of varying aluminum mole fraction as the etch-stop material in conjunction with a buffered citric acid or succinic acid solution as the etchant. This approach typically requires Al mole fraction of 0.35 to 1.0 in order to achieve adequate selectivity. However, the inclusion of a thin AlAs or high

mole fraction $Al_xGa_{1-x}As$ layer into the epitaxial structure will disrupt the flow of current through the material, causing an increase in the ohmic contact resistance and adding to the source resistance of the device. This effect is particularly severe for AlAs, which has shown to increase the contact resistance 67% (from 0.15Ω-mm to 0.25Ω-mm) for the inclusion of a 10Å layer into a MESFET structure [2]. Furthermore, the use of moderate Al mole fraction etch-stop layers (x~0.35) requires very tight control over the Al content to ensure long term process reproducibility as it directly influences the selectivity of the buffered citric acid etch solution [3].

To overcome the shortcomings of the $Al_xGa_{1-x}As$ and AlAs approaches, we have developed an advanced selective gate recess process using $In_{0.5}Ga_{0.5}P$ as the etch-stop layer. In comparison to AlAs, $In_{0.5}Ga_{0.5}P$ has a smaller conduction band offset (0.18eV vs. 0.50 eV) and exhibits no deleterious effects on ohmic contact and FET source resistance. Additionally $In_{0.5}Ga_{0.5}P$ utilizes simple H_2SO_4:H_2O_2:H_2O etch chemistry to achieve greater than 150:1 GaAs:$In_{0.5}Ga_{0.5}P$ etch selectivity. This process has been successfully incorporated into multiple PHEMT layer structures used to fabricate high performance MMICs from 1 to 40 GHz.

$In_{0.5}Ga_{0.5}P$ Etch-stop Approach

A generic PHEMT layer structure showing the inclusion of an $In_{0.5}Ga_{0.5}P$ etch-stop layer is depicted in Figure 2. For this work, the etch-stop layer was interposed between the AlGaAs schottky layer and the n+ GaAs contact layer. To assess the affect of $In_{0.5}Ga_{0.5}P$ incorporation on ohmic contact resistance, $In_{0.5}Ga_{0.5}P$ layers of two different thickness' (35 Å, 50 Å) were inserted into a standard PHEMT layer structure and ohmic contacts formed using standard Au/Ge metallurgy. After isolation, the contact resistance was measured using the TLM method. The results of these measurements are shown in Figure 3. Also shown in this figure are contact resistance values for a PHEMT layer structure containing 2 separate 35 Å $In_{0.5}Ga_{0.5}P$ layers. This was evaluated in anticipation of a fully selective double recessed PHEMT. From Figure 3, one observes that, in comparison to the control group (i.e. non etch-stop) the insertion of a 35 Å layer has no effect on the contact resistance while the 50 Å layer results in a slight increase of 0.015 Ω-mm. This figure also shows that the insertion of two 35 Å $In_{0.5}Ga_{0.5}P$ layers does increase the contact resistance values (from 0.045 to 0.086 Ω-mm), however this higher value is well within the process specification and is not expected to deteriorate device performance. From these data, we draw the following conclusions: 1) A 35 Å

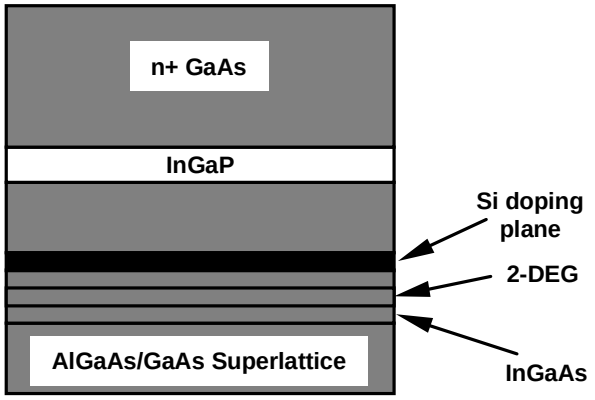

Figure 2 PHEMT layer structure with InGaP etch-stop

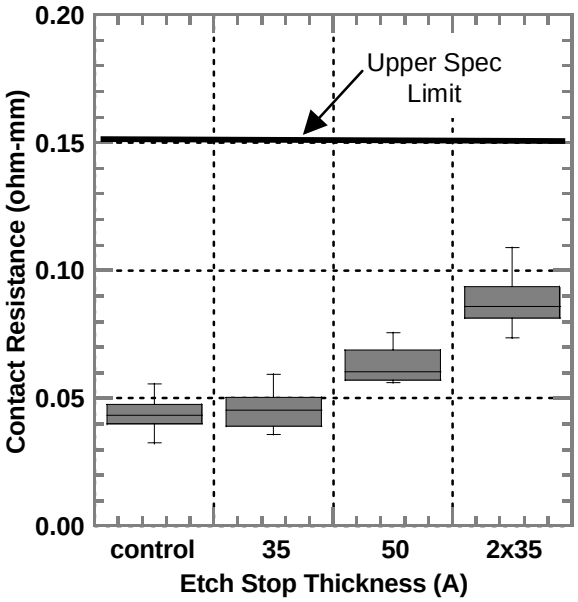

Figure 3. Contact resistance on PHEMT material incorporating various InGaP etch-stop layers

etch-stop layer is preferable since it has no affect on contact resistance and, 2) Despite a substantial increase in ohmic contact resistance for the double etch-stop PHEMT layer structure, the contact resistance values obtained are well in specification making the double etch-stop a viable approach.

Etchant Selectivity

To obtain adequate selective etch behavior, the GaAs/$In_{0.5}Ga_{0.5}P$ selectivity was evaluated for a number of different recess solutions [2]. Selectivity was determined by subjecting patterned samples with thick $In_{0.5}Ga_{0.5}P$ layers to long etch times followed by depth measurements via profilometry. We have determined that a 1:8:500 H_2SO_4:H_2O_2:H_20 etch solution provides a GaAs/ $In_{0.5}Ga_{0.5}P$ selectivity of 150:1 and possesses a manageable GaAs etch rate of 10-15 Å/second. This selectivity coupled with a moderate etch rate is quite different than the citric and succinic acid solutions which typically have GaAs etch rates in the range of 30–50 Å/second. The advantage of a lower GaAs etch rate is that it enables one to more precisely control the extent of lateral etching once the recess terminates at the stop layer. Excessive lateral etching will cause an increase in the source resistance of the device which, if too severe, will degrade noise and power performance.

The selective behavior of the H_2SO_4:H_2O_2:H_20 etch coupled with the $In_{0.5}Ga_{0.5}P$ etch-stop is demonstrated in Figure 4, which is a plot of the ungated drain current vs. etch time for a 0.2x100 μm Low Noise PHEMT. This plot shows the etch terminating at 30 seconds with little change in drain current until 180 seconds of total etch time. This characteristic demonstrates more than adequate selectivity and process latitude for use in manufacturing. Upon completion of the selective etch, the $In_{0.5}Ga_{0.5}P$ layer is removed using a 1:1 HCl:DI solution enabling the schottky to be formed to the underlying AlGaAs. Use of this solution, which exhibits infinite $In_{0.5}Ga_{0.5}P$:AlGaAs selectivity, results in the DC characteristics of the PHEMT (Idss, Vp, g_m etc.) to

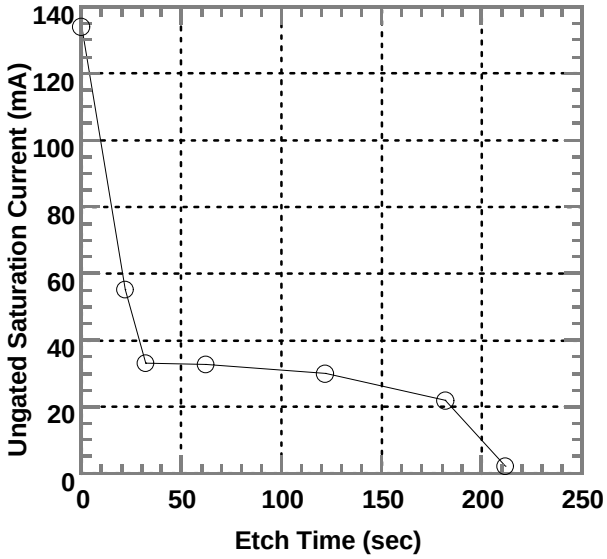

Figure 4. Ungated drain current vs. etch time for a LN PHEMT structure with a 35 Å InGaP etch-stop layer

be determined by the properties of the 2-DEG and AlGaAs thickness and uniformity.

Impact on Device Characteristics

The prime concern over the use of the $In_{0.5}Ga_{0.5}P$ etch-stop process was the potential increase in PHEMT parasitic source resistance (R_s) and associated performance degradation. For any etch-stop process, an increase in R_s can arise from perturbation of current flow by the etch-stop layer and/or excessive lateral etching after the recess etch has terminated at the stop layer. To examine this, Figure 5 shows a plot of the low field on resistance (R_{on}) as a function of I_{dss} for 0.5x200μm PHEMTs fabricated with and without the $In_{0.5}Ga_{0.5}P$ etch-stop. PHEMT R_{on}, which is a measure of all the parasitic resistances from the source to gate, is of particular interest as it directly relates to the insertion loss of the device when used in control applications. In Figure 5, one observes that the R_{on} values for the etch-stop devices are nearly the same as the non etch-stop. In fact, for the typical I_{dss} range for the process (200-350 mA/mm), the etch-stop devices exhibit slightly lower values of R_{on}. This behavior provides evidence that the inclusion of the

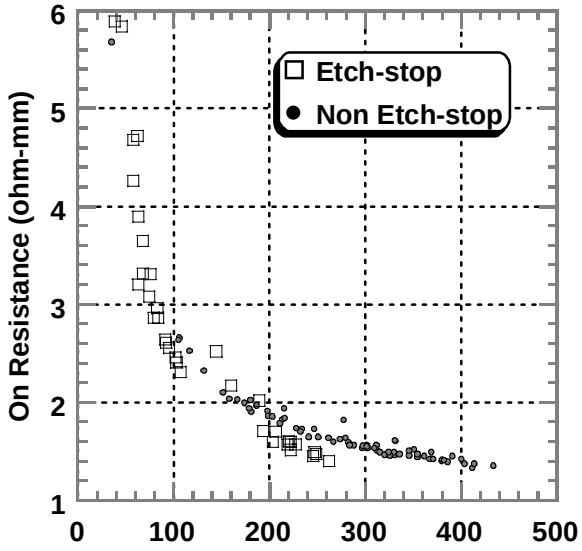

Figure 5. Ron vs. Idss for standard and $In_{0.5}Ga_{0.5}P$ etch-stop PHEMTs

$In_{0.5}Ga_{0.5}P$ has not increased the access resistance to the channel.

Further evidence of the efficacy of the $In_{0.5}Ga_{0.5}P$ etch-stop process can be seen in Figure 6, which is a scatter plot of extrinsic transconductance (Vds=3, Id=75mA/mm) vs. I_{dss} 0.2x200µm mm-wave low noise PHEMTs. Since PHEMT transconductance is strongly influenced by variations in the spacing between the gate and

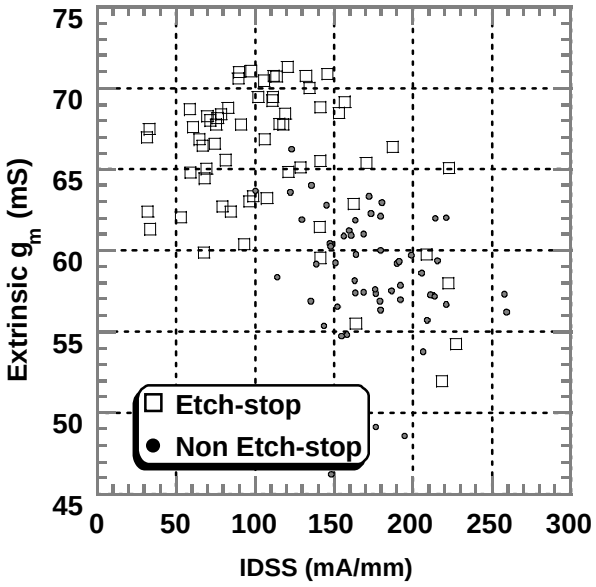

Figure 6 Extrinsic Transconductance vs Idss for 0.2x200 µm mm-wave LN PHEMTs

2-DEG (of which I_{dss} is a good indicator), any comparison of PHEMT g_m must account for this effect. Hence the data is plotted as a function of I_{dss} and shows both device types following the same trend with the etch-stop devices exhibiting generally higher extrinsic g_m in the 120-200 mA/mm range. Since the calculation of extrinsic g_m takes the source resistance into account, one concludes that the implementation of the $In_{0.5}Ga_{0.5}P$ etch process has not degraded the source resistance. This result further demonstrates the superiority of this technique when compared to approaches that employ AlAs or high Al mole fraction AlGaAs etch-stop layers.

Conclusions

An advanced selective gate recess etch process utilizing $In_{0.5}Ga_{0.5}P$ as the etch-stop layer has been developed and incorporated into PHEMT manufacturing. This approach employs conventional H_2SO_4:H_2O_2:H_20 etch chemistry and exhibits a GaAs: $In_{0.5}Ga_{0.5}P$ selectivity of 150:1. Furthermore, this high selectivity is obtained with a moderate GaAs etch rate which reduces the extent of lateral etching during the gate recess process. PHEMTs fabricated with 35Å $In_{0.5}Ga_{0.5}P$ etch-stop layers do not exhibit degradation of DC and RF characteristics when compared to non etch-stop devices. The $In_{0.5}Ga_{0.5}P$ etch-stop process has been incorporated into AMP-M/A-COM's baseline 0.5µm and 0.2µm PHEMT processes.

References:

[1] D. Danzilio, B. Lauterwasser, M. Schneider "Effects of Material Variations on the Gate Recess Behavior of Pseudomorphic HEMTs", Proc. 1994 U.S. Conference On GaAs Manufacturing Technology, p. 53

[2] A.W. Hanson, D. Danzilio, K. Bacher, L. Leung "A Selective Gate Recess Process Utilizing MBE Grown $In_{0.5}Ga_{0.5}P$ Etch-Stop Layers For GaAs-Based FET Technologies" Proc. 1998 GaAs IC Symposium, p. 195.

[3] B. C. Schmukler, P. E. Brunemeir, W. R. Hitchens, D. B. Cantos, W. A. Strifler. D. H. Rosenblatt, R. D. Remba, "Highly Selective Citric Buffer Etch-Stop Process for the Manufacture of Very Uniform GaAs/AlGaAs FETs" Proc. 1993 GaAs IC Symposium, P.325

[4] T. Kitano, S. Izumi, H. Minami, T. Ishikawa, K.Sato, T. Sonoda, M. Otsubo, "Selective Wet Etching for Highly Uniform GaAs/$Al_{0.15}Ga_{0.85}As$ Heterostructure Field Effect Transistors" J. Vac. Sci. Technol. B 15(1), 167, (1997)

[5] T. P. E. Broekaert, C. G. Fonstad, "AlAs Etch-Stop Layers for InGaAlAs/InP Heterostructure Devices and Circuits", IEEE Trans. Electron Devices, vol. 39 no. 3 p. 533