Accelerated Lifetests for High-Speed 0.5-μm InGaAs PHEMT Switches

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ABSTRACT

AlGaAs/InGaAs pseudomorphic high electron mobility transistors (PHEMT) represent a significant technology and performance advancement compared with traditional GaAs HEMTs and MESFETs. High reliability is a critical requirement for their device applications. M/A-COM has conducted accelerated lifetests on hundreds of PHEMT MMIC switches, using high-temperature reverse biased stress (HTRB) at 225 and 250°C, and unbiased stress at 200, 225, and 250 °C. While some change was observed in the DC characteristics, there was almost no degradation in the switch RF S-parameters after 3,000 hours of stress. A worst-case statistical analysis, using typical values for the lognormal failure distribution parameters and activation energy, projected a mean lifetime of over 10^6 hours at 125°C, suggesting highly reliable performance. The transmission electron microscopy (TEM) images showed evidence of gate-sinking failure mechanism, believed to be responsible for the observed gradual degradation in device DC characteristics.

INTRODUCTION

PHEMTs have demonstrated superior MMIC performance up to millimeter-wave frequencies for a variety of commercial wireless communication and military applications [1]. The cost of PHEMTs is now comparable to that of MESFETs due to the maturation of PHEMT manufacturing technology over the last few years, and the reduction in starting substrate costs. However, the understanding of PHEMT reliability, a key requirement in the success of both commercial and military missions, has not yet reached this same level of maturity. Because PHEMT has more complex material structure compared with MESFET, there have been increasing interests and efforts in assessing the PHEMT reliability and identifying its various failure mechanisms [1-4].

Semiconductor devices usually last for many years under normal use conditions. However, product reliability information must be quickly generated for management and engineering decisions to address today's rapidly changing market opportunities. Such information can be quickly obtained using accelerated testing techniques, in which devices are subjected to higher-than-normal stress levels, leading to failure within weeks or months rather than years. By fitting this accelerated failure data to an appropriate model, product reliability under normal use conditions can be estimated.

M/A-COM has recently developed a low cost, manufacturable 0.5-μm InGaAs PHEMT process for switch and amplifier products used in high-volume cellular handset and radar applications. Accelerated lifetests under electrical and/or thermal stresses have been performed. DC and RF parametric degradation has been monitored over the stress period. Both statistical and physical failure analyses have been performed.

DEVICE STRUCTURE AND CIRCUIT

The PHEMT heterojunctions are epitaxially grown using molecular beam epitaxy (MBE) technology. An undoped InGaAs layer is used as a channel to conduct the 2-dimensional electron gas. A superlattice buffer (alternating thin layers of GaAs/AlGaAs) beneath the channel is used to enhance the charge confinement which produces a sharp pinch-off and high transconductance. "Double-pulse" doping planes are placed on both sides of the channel to increase the carrier density (~3×10^{12}/cm^2) with a mobility greater than 6500 cm^2/V-s at 300 K. Ti/Pt/Au gates are defined over the AlGaAs layer by a double-recess process to maximize the breakdown voltage. Drain and source ohmic contacts are formed over the n^+-GaAs cap.

The test vehicle (Fig. 1) is Single Pole Double Throw (SPDT) switch consisting of four FETs, each having four 0.5-μm gate fingers and a total gate width of 0.5 mm. As shown in Fig. 2, these devices exhibited high break down voltage (> 18 V), high transconductance (350 mS/mm), small gate leakage current (1μA/mm), low insertion loss (~0.6 dB), and high isolation (>35 dB) near 1 GHz. Typical values of other parameters are pinch-off voltage V_p = 0.7 V, I_{dss} = 200 mA/mm, and on resistance R_{on} = 2 Ω·mm. Two series FETs (Q2 & Q3) provide a through path for the "on" arm while the shunt FETs (Q1 & Q4) provide isolation for the "off" arm [5]. The series resistors can improve device isolation and act as current limiters. Table 1 summarizes the switch logic.

TABLE 1
TRUTH TABLE FOR SPDT SWITCH (LOW: 0 V. HI: -3 to -5 V.)

Control Input		RF COM to each RF Port	
VA	VB	RF1	RF2
HI	LOW	ON	OFF
LOW	HI	OFF	ON

ACCELERATED LIFETEST PROCEDURE

240 PHEMT switches were randomly selected from two wafers. Each wafer consisted of devices with two different

ohmic contact widths (5 μm and 15 μm). Each of these four groups of devices was divided into six subgroups for various constant stress levels under high temperature reverse bias (HTRB) at 225 and 250 °C, or unbiased storage at 200, 225, and 250 °C. Ten unstressed devices from each group were saved as control samples for measurement calibration. HTRB test was chosen because it most closely matches the switch normal use condition, where there is almost no DC power dissipation. A -4 V (~$6V_p$) bias was applied to the gates of all FETs. The gate leakage current, temperature, and bias voltage of each device were continuously monitored and recorded using a computer automated data acquisition system.

Figure 3 plots the *in-situ* gate current I_g monitored during the HTRB burn-in stress. The change was moderate and less remarkable than that observed in the earliest study of M/A-COM MESFET switches [6].

EXPERIMENTAL RESULTS

The stresses were periodically removed for a series of RF and DC characterizations at room temperature to monitor device degradation. Figure 4 shows the RF and DC parametric degradation over time after HTRB stress up to 3,030 hours for one selected group. Other 3 groups exhibit similar changes. Unbiased storage (thermal stress only) results in a smaller degradation, suggesting that electrical stress may induce additional failure mechanisms. The degradation rates are comparable with that in M/A-COM's recent recessed gate MESFET process [4].

Little difference in degradation is seen between 225 and 250 °C. One should be cautious not to conclude that the devices have a low activation energy (E_a). The degradation is not significant enough at either temperature to allow us to accurately calculate E_a. Although the degradation in DC parameters (V_p, R_{on}, or I_{dss}) is moderate (5–10%), the change in RF insertion loss, a primary parameter of interest in switch applications, is never greater than 0.1 dB (or < 2% degradation in power loss). Our high power measurements demonstrated little degradation in insertion loss up to 25 dBm input power, and the 1 dB compression is at 29 dBm or 0.8 W.

LOGNORMAL STATISTICS AND ARRHENIUS ANALYSES

The little degradation under such reasonably high stress level (250°C over 3,000 hours) indicates PHEMT can be highly reliable. Given the limited change and lack of failures observed, it is difficult to accurately calculate reliability parameters such as failure rate, mean-time-to-failure (MTTF), and activation energy. Nevertheless, we can proceed to perform a worst-case assessment as follows.

Lognormal statistics are generally accepted for semiconductors devices. The probability density function PDF for a lognormal failure distribution is defined as [7]:

$$\text{PDF} = f(t) = \frac{1}{\sigma\, t\sqrt{2\pi}}\, e^{-\frac{1}{2}\left(\frac{\ln t - \ln t_{50}}{\sigma}\right)^2} \qquad (1)$$

where t_{50} is the median failure time and σ the shape parameter. The MTTF according to Arrhenius equation is:

$$\text{MTTF}(T) = t_{50}\exp\left(\sigma^2/2\right) = A\exp\left(E_a/kT\right) \qquad (2)$$

Throughout our 3030-hour stress tests, no failures have been observed. We conservatively assume that the first failure occurs right after 3,030 hours at 250 °C. Using a typical value for σ = 0.5 and according to Eqs. (1) and (2), we obtain

$$t_{50} = 8{,}236 \text{ hours} \quad \& \quad \text{MTTF} = 9{,}333 \text{ hour} \qquad (3)$$

at 250 °C. The calculated t_{50} (50% failure) is about 2.7 times the total stress period and may serve as a reasonably conservative estimate.

Given MTTF at 250 °C, we can compute MTTF at various temperatures as listed in Table 2 for three selected values of E_a. Furthermore, we project the instantaneous failure rate (IFR) in Table 3.

TABLE 2
MTFT AT VARIOUS TEMPERATURES (σ = 0.5)

E_a (eV) =	0.7	1.0	1.3
T(°C)	MTTF (Hours)		
250	9,333	9,333	9,333
125	1.2×10^6	9.9×10^6	8.0×10^7
85	1.2×10^7	2.6×10^8	5.6×10^9
50	1.4×10^8	8.7×10^9	5.3×10^{11}

TABLE 3
INSTANTANEOUS FAILURE RATE (E_a = 0.7 eV, σ = 0.5)

	10 Years	15 Years	20 Years
T(°C)	IFR (FITs)		
150	300	1242	2405
125	0.03	0.84	6.0
100	$< 1\times10^{-5}$	$< 1\times10^{-5}$	1×10^{-5}

We believe the above results represent the best minimum reliability estimate of our current PHEMT process. While the temperature limits for military and commercial applications are 125 and 85 °C, respectively, the operation condition is often around or below 50 °C since almost no self–heating occurs in switch applications. The lifetime is predicted over 10^8 hours at 50 °C in the worst case.

FAILURE ANALYSIS

The electrical results in Fig. 4 show a degradation of reduced V_p, increased R_{on}, and declined I_{dss}— indicative of "gate sinking" mechanism due to gate metal migration into the GaAs material. Another commonly reported failure mechanism, called ohmic contact degradation (normally manifesting itself by degradation in I_{dss} and R_{on} but NOT in V_p), is unlikely or secondary in our devices.

To confirm this mechanism, cross-sectional transmission electron microscopy (TEM) images were taken near the interface of gate metal and semiconductor layers. As illustrated in Fig. 5, the stressed device exhibits a strain field extending into the AlGaAs/InGaAs region. This strain field is caused by metal diffusion or "gate sinking." It results in a reduction of effective channel thickness, carrier concentration, or electron mobility, leading to a decreased V_p, I_{dss}, and enhanced R_{on}. Our recent analysis suggests this mechanism has high activation energy.

SUMMARY

We have conducted reliability lifetests on M/A-COM's recent PHEMT switch process at elevated temperatures. The primary failure mechanism is gate-sinking. The projected mean lifetime of over 10^8 hours at 50 °C suggests this PHEMT device technology has a highly reliable performance comparable with that of the MESFETs in meeting the requirements of demanding microwave switch applications.

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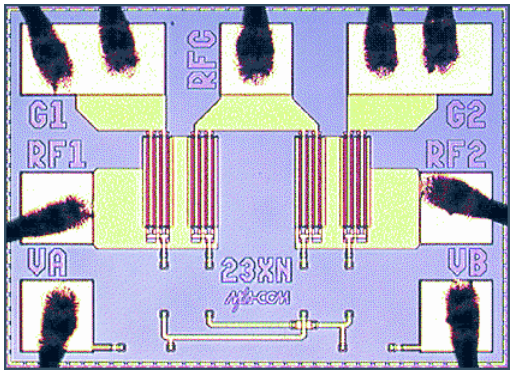

Fig. 1. PHEMT SPDT switch photograph and circuit schematics

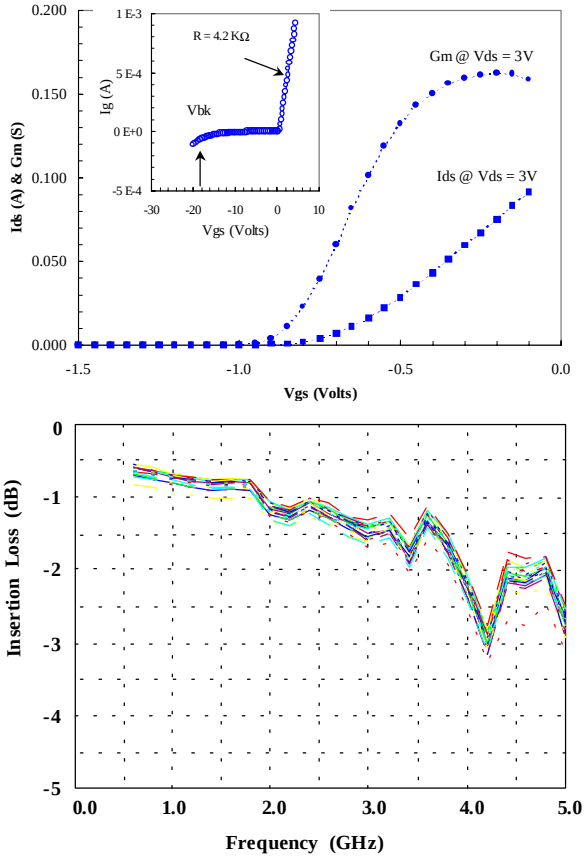

Fig. 2. Top panel: Transfer characteristics, showing a peak transconductance of 320 mS/mm; the inset plots the diode curve showing a breakdown V_{bk} > 20 V. Bottom panel: RF insertion loss over 0.5–5 GHz in small signal S-parameter measurements for 30 PHEMT switches—10 unstressed samples and 20 HTRB stressed devices for 2,100 hours at 225 and 250°C.

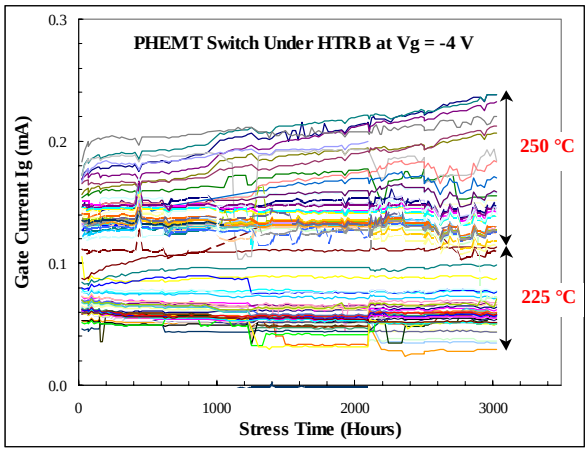

Fig. 3. *In-situ* gate current measured while devices (80 PHEMTs) were under HTRB stress at 225 and 250 °C.

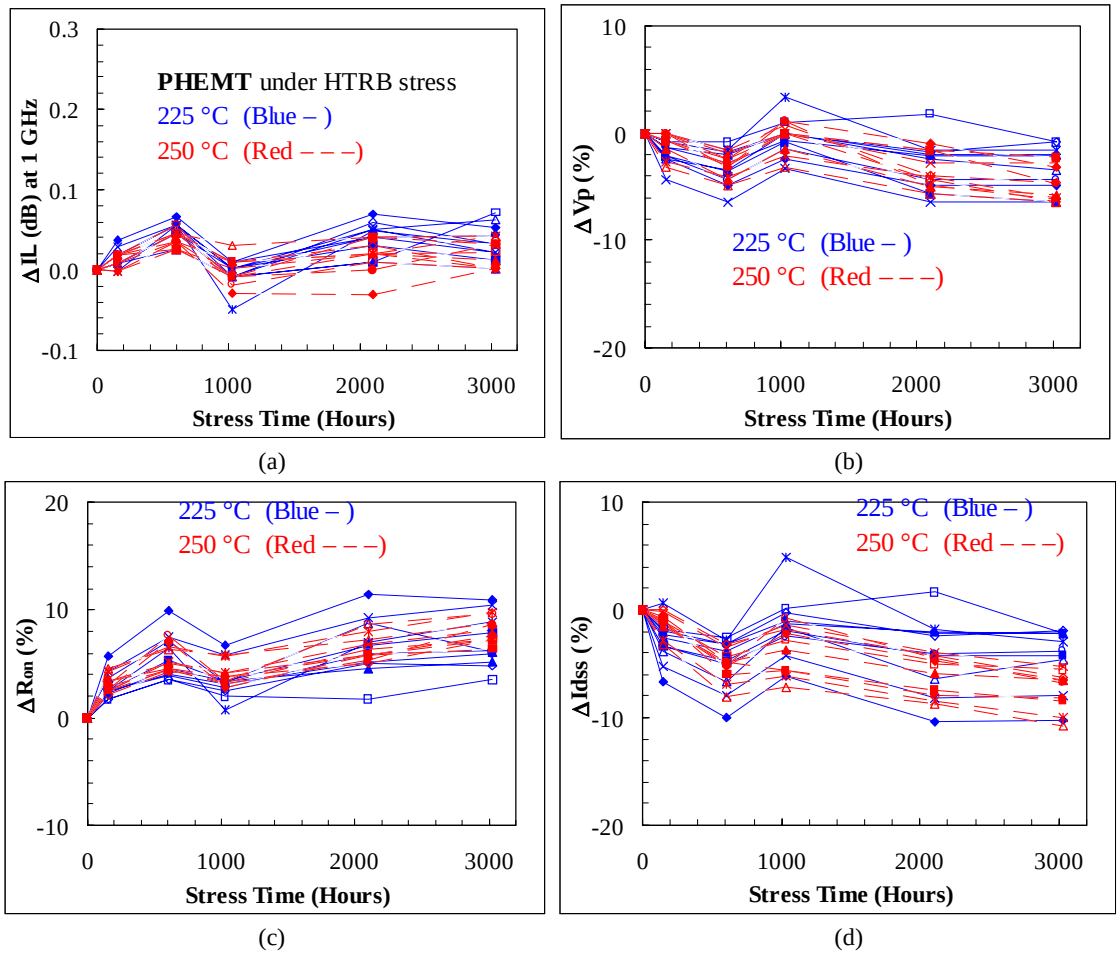

Fig. 4. Change of RF loss in dB and percentage change of primary DC parameters measured at room temperature over the elapsed HTRB stress at 225 (solid lines) and 250 °C (dashed lines): (a) Small-signal insertion loss at 1 GHz, (b) Pinch-off voltage, (c) Channel on-resistance, and (d) Drain saturation current.