A Two Step Polyimide Etchback for Integration of Heterojunction Bipolar Transistors and Resonant Tunneling Diodes

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Abstract

A process is reported on for integration of resonant tunneling diodes (RTDs) and heterojunction bipolar transistors (HBTs.) Single stacked layer growth, etch stop layers, in situ sensors, and simulation have been used to improve and ensure the manufacturability of the process. Only minor modifications to the existing HBT process were required to incorporate the RTDs.

Introduction

Resonant Tunneling Diodes have been used to improve circuit performance by reducing transistor count and power dissipation.[1, 2] Integration of RTDs with Heterojunction Bipolar Transistors (HBTs) is of interest for high speed, low power logic gates.[3] RTDs integrated with the baseline HRL HBT IC process have been demonstrated previously using MBE growth on patterned InP substrates.[4] The process described here begins with a stacked MBE growth on a planar, epi-ready substrate.[5] This process is readily manufacturable as there are only two additional process steps required to incorporate RTDs into the standard HBT IC process.

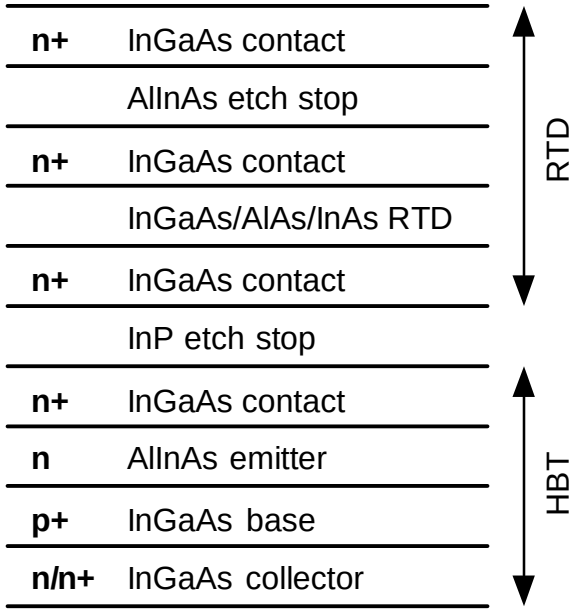

Fig. 1. Epitaxial layer structure for integrated HBT-RTD process. Note the use of etch stop layers for manufacturability.

Experiment

The GaInAs/AlInAs-based HBT layers are grown first on an InP substrate and then the InGaAs/AlAs/InAs RTD layers are grown on top of the HBT layers. The two devices are separated by an InP etch stop layer to distinguish the HBT emitter cap from the bottom contact of the RTD. Eliminating the regrowth step and making use of etch stop layers simplifies the process. Figure 1 shows a simplified schematic of the overall epitaxial structure including InP and InAlAs etch stop layers.

The layers were grown in an MBE system with *in situ* sensors for layer thickness and substrate temperature control.[4] A photoemission oscillation sensor is used to control the AlAs barrier thickness that is critical for achieving the designed peak current values for the RTDs. A transmission-mode absorption-edge spectroscopy sensor controls the substrate temperature to a precision of $\pm$ 1 ^{o}C throughout the growth.

The first additional step to the baseline HBT IC process involves patterning and etching the RTD mesa region. The area outside the RTD mesa is etched to the InP etch stop layer, which is then removed to expose the HBT emitter cap layer. HBT processing proceeds from this point with the emitter metal serving as both the HBT emitter contact and the top contact of the RTD.

Next, the emitter and top contact of the RTD are etched and base metal is deposited. The base metal contacts both the HBT base layer and the

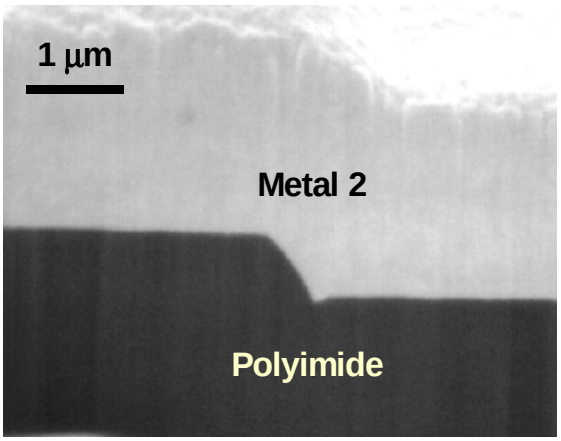

Fig. 2. Cross-sectional SEM of second-level metal step coverage at RTD mesa edge.

bottom layer of the RTD. One modification to the RTD structure was made to facilitate this procedure. A thin AlInAs etch stop layer was inserted in the RTD top contact 100 nm below the surface. In the standard HBT process, a 100 nm n^+-GaInAs emitter cap layer is removed using a $CH_4/H_2/Ar$ reactive ion etch (RIE). This etch is selective to the underlying AlInAs emitter layer and effectively stops on this layer. This allows overetching of the wafer to ensure etch depth uniformity across the wafer. By inserting an AlInAs etch stop layer in the top contact of the RTD, both devices have an etch stop layer and the standard RIE process can be used. After the RIE, a non-selective wet etch is used to etch to the base layer of the HBT. This also etches through the RTD active layers into the bottom contact layer.

The second additional step for fabrication involves planarization and interconnect. In the baseline HBT IC process, polyimide is spun on the wafers and etched back to expose the emitter metal.[6] An inductively coupled plasma (ICP) system is used to etch the polyimide with O_2. The etch system is equipped with a laser reflectometer for process control of polyimide etch depth.

Due to the stacked layer growth, the top contacts of the devices are non-planar. A two step polyimide etchback has been developed. For the combined HBT plus RTD process, the top contact of the RTD is the highest metal layer on the wafer, and the first to be exposed during polyimide etchback. To prevent removal of polyimide over the bottom contact of the RTD, the etch is stopped prior to exposure of the HBT emitter metal.

After the first planarization etch, the RTD mesa is masked with photoresist. The etchback is continued with an O_2/Ar plasma to remove polyimide above the HBT emitter contact. The addition of Ar to the plasma causes a tapered polyimide profile at the RTD mesa edge.[6] This allows second level metal to cross this edge and interconnect the RTDs with the HBTs and other circuit elements. A cross-sectional scanning electron micrograph of the mesa edge is shown in Fig. 2. The cross-section was cut using focused ion beam milling. After the second etchback step, both of the top device contacts are clear and can be contacted by second level metal.

Process simulation was used to ensure first pass success. Figure 3 is a simulation generated cross-section of an HBT connected by second level metal to an RTD. The simulation tools used were Technology Computer Aided Design (TCAD)

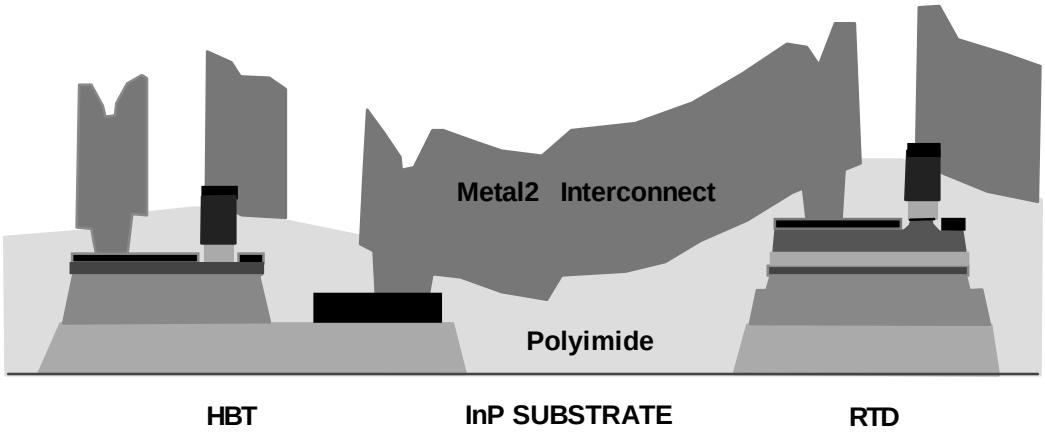

Fig. 3. Simulated cross-section of HBT and RTD showing interconnection of devices. The vertical scale has been expanded to show more detail.

software packages designed to model silicon IC fabrication. Due to the use of liftoff technology in our process, the sequence was modified to allow the TCAD tools to accurately model the metalization steps.[7]

Results

The simulation software generated cross-sectional views of the wafer at different stages of the process. This aided in the development of the RTD epitaxial structure. The thickness of the bottom contact layer needs to be at least a certain value set by the maximum current through the device. Simulation allowed investigation of using various bottom contact thickness and implications to the process. In this way, the bottom contact layer was set at 400 nm.

Simulations were used to predict target values for the polyimide etchback step. The metal step coverage over polyimide shown in Fig. 2 can be seen in the simulated cross-section of Fig. 3. The simulation divided the normal polyimide etch-back into two steps. In the first step, 4/7 of what is removed in the baseline process is etched. Then, the RTD is masked and the remaining polyimide over the HBTs is etched. The simulation shows a step of ~500 nm at the edge of the RTD mesa. It also shows that both top contacts of the devices are cleared from the polyimide. The mask is the same used in the first step to define the RTD mesa such that only one additional mask is required to include RTDs in the HBT IC process.

The benefit of the two step etchback approach is that it allows both devices to be patterned with the minimum design dimensions. Had only the RTD contact been exposed, a via would have to be etched to the HBT emitter. This would require a larger emitter area to contain the via. By etching back and exposing both top contacts, both the HBT and RTD can have minimum area contacts. This reduces the required current and power dissipation for each device.

Another step that benefited from simulations was the isolation etch step. The simulations indicated a need for an increased etch time due to the stacked layer growth. Figure 4 shows how the RTD mesa would look after the standard isolation etch from the HBT process. It can be seen that when the HBTs are completely isolated, there is still collector material within the RTD mesa equal in thickness to the RTD epitaxial layer stack. Therefore, the isolation etch time is increased to remove this material, isolate the RTD mesa, and eliminate this step at the mesa edge.

After fabrication was completed, the standard automated test routine was performed. The transistor array yields for the combined HBT-RTD process were comparable to those for the baseline HBT IC process. Figure 5 shows an example I-V curve for a 2x5 μm^2 emitter HBT. The small bandgap of the GaInAs base material and the graded base-emitter junction results in a low turn-on voltage of the device. This also allows lower power operation compared to GaAs-based HBT ICs.

Figure 6 shows an example I-V curve for the finished RTD device. The area of the top contact of the RTD was also 2x5 μm^2. The peak current was 4 mA, (or $4x10^4$ A/cm^2) at 200 mV.

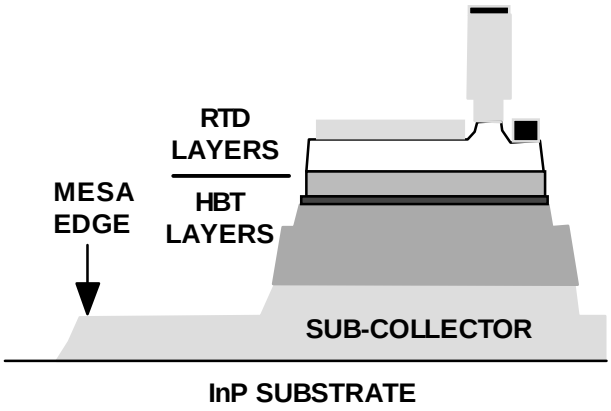

Fig. 4 Simulation of RTD after standard HBT isolation process, showing need for additional device isolation.

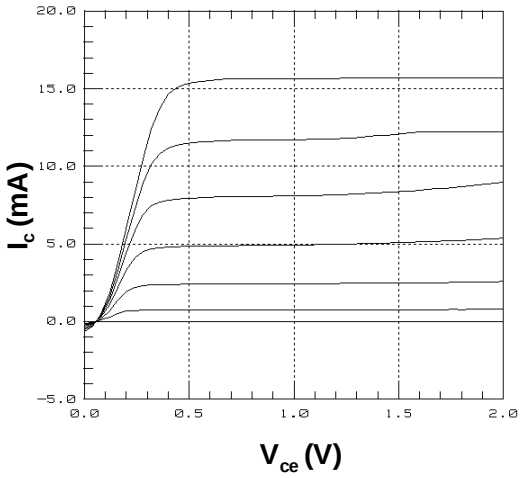

Fig. 5. Collector current plotted versus collector-emitter voltage for 2x5 μm^2 emitter HBT.

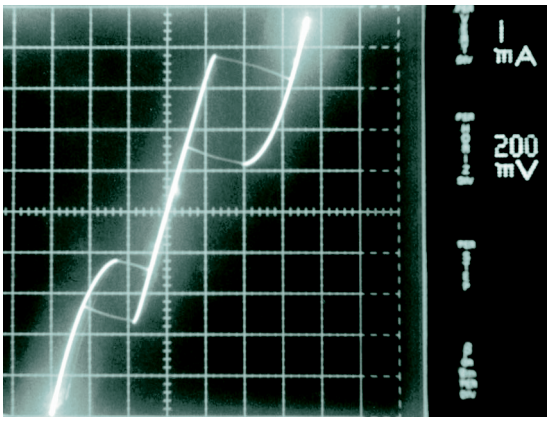

Fig. 6. I-V characteristic for 2x5 μm^2 RTD.

Figure 7 shows a photograph of a typical finished circuit topology. An RTD mesa is shown that contains six RTDs of varying dimension. Also shown are 2x10 μm^2 emitter HBTs and a pair of thin-film resistors. Not shown, but also supported by the IC process, are dielectric capacitors and spiral inductors.

Conclusion

A process has been developed for integration of HBTs and RTDs. Manufacturability was considered at each step of the process. Critical fabrication steps employed either in situ sensors or etch stop layers for process control. Only minor modifications to the existing baseline HBT IC process were made and only one additional mask was required. Definition of an RTD mesa allowed both devices to be patterned simultaneously. A two-step polyimide etchback provided direct access to both device contacts. Vias were etched to the remaining contacts. Process simulation was used to study the impact of the changes and determine process parameters such as etch depths and layer thicknesses.

Acknowledgments

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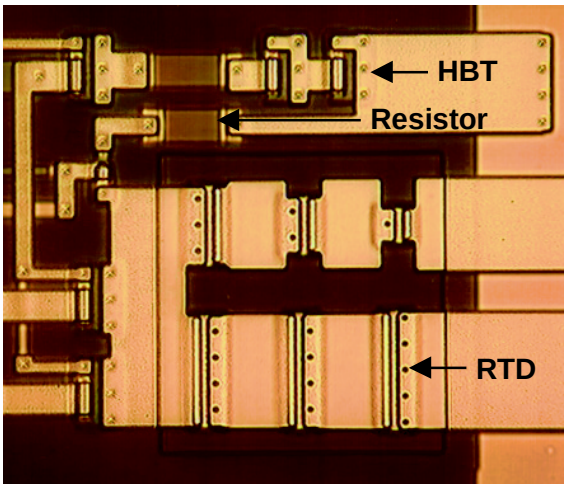

Fig. 7. Photograph of a portion of an IC showing RTDs integrated with HBTs.

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