Electrochemical Etching in the Fabrication of Short Gate-Length InAlAs/InGaAs Heterojunction FETs

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ABSTRACT

The use of electrochemical etching in fabricating InAlAs/InGaAs heterojunction field-effect transistors (HFETs) is presented. The electrochemical etching arises when resist openings are employed to monitor the drain current of HFETs during wet-chemical gate recess, which results in etching rates for InGaAs and InAlAs that are significantly different from those calibrated with wafer pieces. The electrochemical phenomena are investigated. Their applications in improving layout-independence and short-channel effects of HFETs are shown. In addition, an electrochemical-etching-based manufacturing technology is demonstrated to fabricate high-performance short gate-length enhancement-mode HFETs.

INTRODUCTION

InAlAs/InGaAs-based HFETs, due to their excellent performance, become very important in low noise, high-frequency, and high-speed applications [1-3]. In the fabrication of HFETs, gate recess etching is a very critical step, because the recess groove profile can significantly influence device performance. Usually, the drain current I_{ds} is monitored to achieve a desired depth for gate grooves, and this is done by applying probes to the exposed ohmic electrodes. However, the simultaneous exposure of the ohmic electrodes and gate openings to the etchant induces electrochemical etching of semiconductors under the gate openings, resulting in etching behavior deviating from that calibrated in the absence of electrodes. The awareness of the electrochemical phenomena in the HFET fabrication is important. Because this would help to get rid of the adverse influences at electrochemical origins [4-6], and more importantly, the features of electrochemical etching can be useful to improve the device performance.

ELECTROCHEMICAL ETCHING

Figure 1 shows a schematic view of recess etching with Ni on ohmic electrodes. In this configuration, semiconductors under gate openings are made the anode and the source and drain the cathodes; the electrochemical circuit is completed by the distributed resistors in the etchant and in the epitaxial layers. It can be found that the surface metal of the ohmic

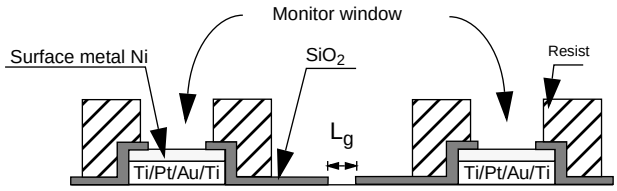

Fig.1: Schematic view of wet-chemical recess etching for HFET fabrication.

electrodes can play a key role in the electrochemical etching in the gate openings. For example, the Ni ohmic electrode surface metal will enhance the etching of semiconductors in the gate grooves by factors of 10 and 4 in the vertical and the lateral directions, respectively, and this forms gate grooves with small side etching. With Pt surface metal, however, etching rates are generally lower and dependent on materials. For heavily doped InAlAs, in particular, etching rate can be even lower than that in the absence of electrodes.

The profiles of gate grooves with different gate lengths have been examined to understand the mechanisms. With Ni electrode surface metal, the longer gate length gives rise to a slower etching; the sample with Pt surface metal, however, just shows the opposite. The obviously accelerated recess etching of the Ni sample, compared with that without the presence of metal, can be explained by the enhancement of oxidation of semiconductors via the electrochemical processes, which are due to the presence of the Ni on ohmic electrodes. Larger gate openings will lead to a decrease in the density of electrochemical etching current in the gate regions, which in turn will result in reduced etching rates. The lower etching rates for the Pt case, on the other hand, are principally due to the excessive oxidation of semiconductors, because Pt has a much higher electrode potential than Ni. The etching is thus governed by diffusion of reacting species.

The awareness of electrochemical effects is essential to fabricating high-performance InAlAs/InGaAs HFETs. An important concern of HFET fabrication is the device scaling in both the gate length L_g and gate width W_g. This is because L_g reduction is essential to enhance the upper limit of operation frequency, and, meanwhile, optimum gate periphery has to be selected for the particular frequency of operation.

IMPACTS OF GATE WIDTH

It is highly desirable for the I_{ds} values of the monitor devices to be as close to the I_{ds} values of the devices in ICs as possible; however, this is not always the case. Figure 2 (short dashed line) shows that the threshold voltage V_{th} of the monitor devices, which have a single finger layout denoted as 1×10 μm (= number of fingers × width of unit finger), is around 0.2 V more negative than the RF devices with a 2×50 μm layout. Even if the total W_g is identical, the resulting performance can differ due to the different etching that occurs during the recess. One can find that the devices having a 4×25 μm layout show a more positive V_{th} than the devices having a 2×50 μm layout. This problem can not be completely solved even with the InP etch stopper (long dashed line), and this should be attributed to the different etching process in the devices with 4×25 μm and 2×50 μm layouts.

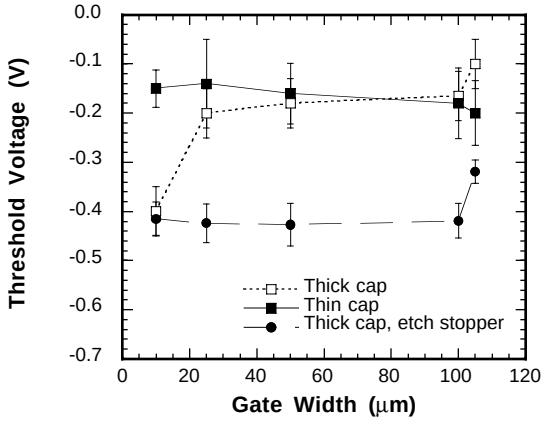

Fig. 2: Threshold voltage versus the total gate width of 0.1-μm HFETs. The W_g of 10, 25, 50, 100, and 105 μm corresponds to with gate layouts of 1×10, 2×12.5, 2×25, 2×50 , and 4×25 μm, respectively.

After studying the etching behaviors for the n^+-InGaAs and n^+-InAlAs, it has become quite clear that the thick cap-layer structure, which is for achieving non-alloyed ohmic contact, contributes significantly to the observed V_{th} discrepancy among devices with different peripheries. This is because different gate layouts lead to different oxidation and therefore etching rates. If the total thickness of the layers removed by recess etching is thick, the difference in etching rates will be "amplified". The methodology we find to be effective is to thin the conventional cap layer structures. This should be much easier and more straight forward than maneuvering the sizes of the monitor windows. All of the thin-cap devices (solid line) demonstrate V_{th} within the range from -0.20 V to -0.15 V, regardless of the number of fingers (1, 2, or 4) and the total gate widths (10, 25, 50, or 100 μm).

SELF-COMPENSATION OF SHORT-CHANNEL EFFECTS

The use of thin cap layer structures allows us to focus on the effects caused by changing the L_g. The HFETs have a 15-nm channel with a $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ structure, in which the 4-nm InAs is inserted at 2 nm from the top of the channel [2], and the device fabrication process has been described elsewhere [3]. The inset of Fig. 3 shows the gate-groove dimensions (depth and width) are dependent on L_g, especially in the sub-0.3 μm regime. Ni surface metal will induce a faster vertical etching in the gate openings that have a shorter L_g. This can be understood from the increase in the electrochemical current density when the L_g decreases. Therefore, the vertical etching in the smaller gate openings will be effectively enhanced in such a self-organized process, resulting in alleviation of the short channel effects. The desirable feature is that this enhanced vertical etching doesn't lead to the same increase in the lateral direction. Furthermore, if the etching time is made longer, gate grooves with smaller L_g will be distinctly deeper and, more importantly, the compensation of short channel effects will become more pronounced.

This actually provides an approach to fabricating HFETs with less severe short-channel effects. Figure 3 does show that the variation of V_{th} with L_g is not monotonic, which should be expected if only short-channel effects considered, and the maximum arises at L_g of around 0.12 μm. This clearly demonstrates that the electrochemical effects should also be taken into account, which is the key to explain the drop in V_{th} at L_g longer than 0.12 μm, though the short channel effects (indicated by the V_{th} shift as large as 250 mV) are still dominant in the shallowly-recessed sample in the sub-0.12 μm regime. But one should be aware that the electrochemical effects are already working to compensate the short-channel effects; were this not the case, the above V_{th} shift in the sub-0.12 μm regime would be even larger. This compensation will become more pronounced when we use a

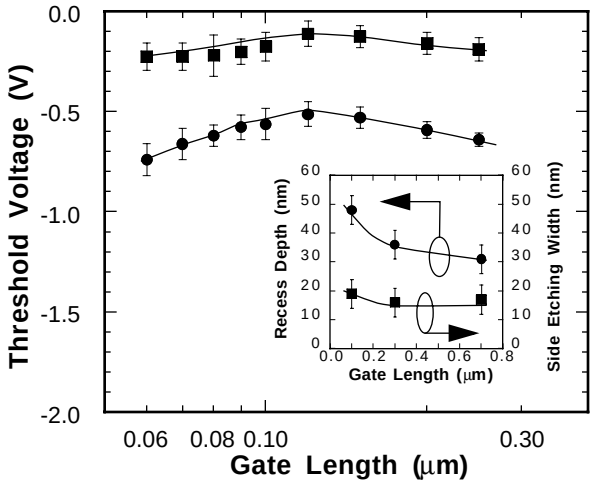

Fig. 3: Threshold voltage (measured at V_{ds} = 1.0 V) of HFETs with L_g ranging from 0.06 to 0.25 μm. The experimental points, indicated with circles and squares, stand for devices with shallow and deep etching, respectively. The inset shows the variations of recess depth and side etching that are induced by the change in gate length.

longer etching time, because this allows the vertical etching enhancement to accrue in the smaller gate openings. This point can be evidenced from the V_{th} shift reduction to 130 mV in the deeply-recessed sample from the original 250 mV.

The alleviated short-channel effects can also be observed in the change of maximum extrinsic transconductance g_m versus L_g, as shown in Fig. 4. One should note that in the case of shallow etching, the decrease in g_m with a reduced L_g is steep below 0.12 μm. This is due to the drain-induced barrier lower in the short L_g devices, as the g_m degradation in the short L_g devices will become more pronounced when a V_{ds} of 2 V is applied. However, when the etching becomes deeper, the electrochemical effects become more pronounced, i.e., the small gate opening produces a distinctly deeper gate groove, resulting in the g_m-L_g curve below 0.12 μm being almost flat. A high transconductance of 1.9 S/mm at a drain bias V_{ds} of 1 V is comparable with that for a 0.1-μm device. This indicates that the deeper etching in the smaller gate openings has effectively alleviated the drain-induced barrier lower in the short L_g devices. At V_{ds} of 2 V, the g_m degradation is obviously less severe, and a record high g_m of 2.35 S/mm has been achieved.

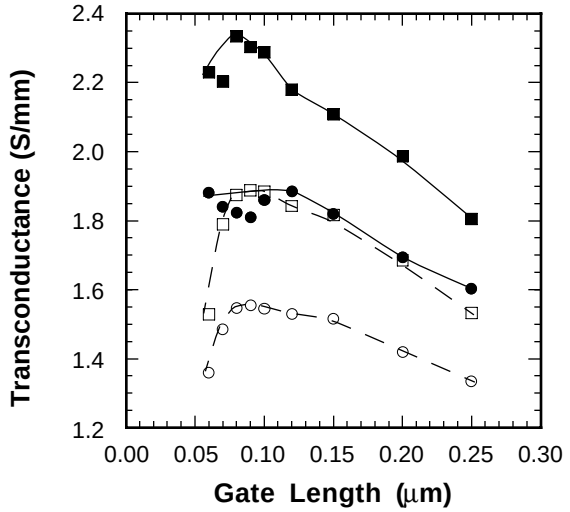

Fig. 4: g_m of HFETs with L_g ranging from 0.06 to 0.25 μm. The experimental points, indicated with open and solid symbols, stand for devices with shallow and deep etching, respectively. Besides, the circles and squares are for the values measured at V_{ds} of 1 and 2 V.

FABRICATING E-MODE HFET

For high-speed applications, direct-coupled FET logic (DCFL) is favored due to its simple circuit configuration. However, the implementation of high-performance enhancement-mode HFETs (E-HFETs) lags far behind that of depletion HFETs. The reasons for this include the large conduction-band discontinuity for InAlAs/InGaAs heterojunction lattice-matched to InP substrates, the lower Schottky barrier on InAlAs, and most importantly, the difficulty in controlling the side etching when deep gate grooves are etched in order to deplete the channel. In particular, when the L_g is reduced to the sub-0.1-μm range to make full use of the excellent transport properties of the InGaAs under a high electric field, the short-channel effects will further push the V_{th} into the negative direction, making it even more difficult. to fabricate E-HFETs.

The geometry features of electrochemical-etching-formed gate grooves, which are described by the inset of Fig. 3, suggest a new approach to fabricating high-performance E-HFETs with ultra-short gate lengths. Because deep groove with very small side etching can be formed with the electrochemical etching, which results in small parasitic resistance and high-performance of devices. The other consideration in the process is the use of 4-nm-InAs-inserted channel with a total thickness as thin as 8 nm to reduce the short-channel effects, which allows the retaining of excellent transport properties [8]. In order to fabricate gate electrodes as small as 0.03 μm, we used a ZEP520with a 10-wt% fullerene incorporation. This composite electron-beam resist has 10-20% higher resistance to the reactive ion etching (RIE) that is used to replicate the gate pattern on SiO_2/Si_3N_4. This makes it possible to use a thinner electron-beam resist, which in turn allows the successful fabrication of gate electrodes as short as 0.03 μm with an accelerating voltage of 25 kV for electron-beam lithography [7]. The other modification to the previous process for fabricating D-HFETs is the use of Pt to replace Ti as the bottom gate-metal layer, as Pt has a 0.15 - 0.20 V higher barrier height on InAlAs than Ti. The use of Pt further shifts the V_{th} upward above zero, and results in the realization of high-performance 0.03-μm InAlAs/InGaAs E-HFETs without using post annealing or two-step gate-recess technologies that were reported previously.

Figure 5 shows the well-behaved transfer characteristics of the 0.03-μm D- and E-HFETs. The Ti gate electrode device demonstrates a V_{th} of -0.3 V, which is extracted by finding the gate bias when $I_{ds}^{1/2}$ is extrapolated to zero. The Pt-based device, which is also a little more deeply recessed, presents a V_{th} slightly above 0 V. This is the first E-HFET with a L_g as short as 0.03 μm. Both devices have very high g_m: 1.86 and 2.05 S/mm for D- and E-HFETs, respectively, with an associated drain current of 0.5 A/mm. The higher g_m for E-MODFET is due to the slightly smaller gate-to-channel separation, which markedly enhances the aspect ratio and, consequently, improves the control of gate over the channel current.

Figure 6 shows excellent *I-V* characteristics of a 0.03-μm E-HFET with good pinch-off behavior. However, at a V_{ds} of 1 V and zero gate bias, the gate leakage current is 0.3 mA/mm. This is basically due to the tunneling current between the gate electrode and the channel, which is obviously enhanced by our employment of the gate-to-channel separation as small as

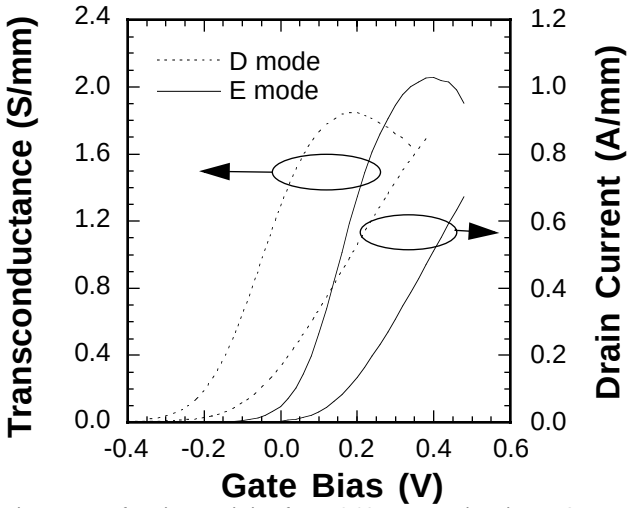

Fig. 5: Transfer characteristics for a 0.03-μm gate length D-MODFET (dashed lines) and a 0.03-μm E-MODFET (solid lines). The devices were biased at V_{ds} = 1.0 V.

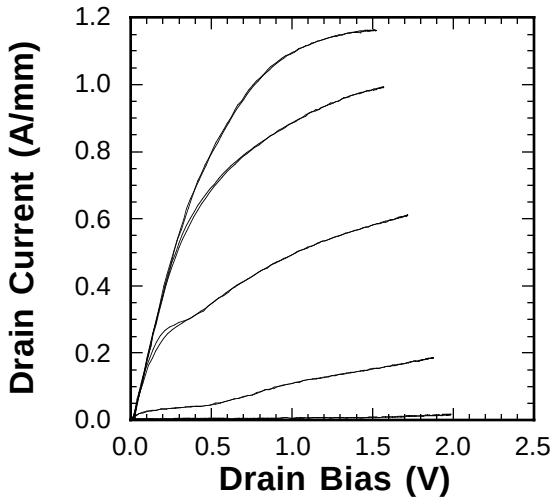

Fig. 6: I-V characteristics of D-MODFETs (a) and E-MODFET (b) with a gate periphery of 0.03 μm × 100 μm. The V_{gs} for the top curves is 0.8 V, and the measurement step of V_{gs} is 0.2 V.

around 10 nm to deplete the channel. The use of barrier materials with a higher band-gap such as tensilely-strained Al-rich InAlAs should be able to improve the gate leakage and makes this electrochemical-etching-based technology more suitable for fabricating high-performance E-HFETs.

This new fabrication technology for E-HFETs should be considered as straight forward and simple compared with the other technologies for E-HFETs, while the control of side etching turns out to be very successful. The resulting parasitic resistance we achieved for E-HFETs is almost the same as that for high-performance D-HFETs. For 0.03 μm devices, as a result, a record high current gain cut-off frequency exceeding 300 GHz has also been achieved at 0.9 V drain bias. The excellent high-speed performance of E-HFETs, together with that of depletion mode devices, provides possibility of realizing ultrahigh-speed circuits based on DCFL with InAlAs/InGaAs HFETs.

CONCLUSIONS

The existence and importance of electrochemical effects in the HFET fabrication process have been shown. We have also studied the major effects of varying gate geometries on the performance of InAlAs/InGaAs-based HFETs, which are at the origin of the electrochemical effects during gate recess etching. With the understanding of these effects, short gate-length HFETs with excellent performance have been fabricated that show high W_g independence insignificant short-channel effects. The electrochemical etching is also used to fabricate slender gate grooves for E-HFETs with gate length as short as 0.03 μm. The low parasitic resistance of 0.03-μm E-HFETs leads to record high extrinsic transconductance of 2 S/mm and f_T exceeding 300 GHz. This opens up possibility for further improvement in high-speed ICs.

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