Effects of Selective Gate Recess Etching on the Static and Microwave Properties of InGaP/InGaAs PHEMTs

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ABSTRACT

$In_{0.49}Ga_{0.51}P/In_{0.20}Ga_{0.80}As$ PHEMTs on a GaAs substrate were fabricated using a selective wet etch process for the gate recess. The recess width was varied by changing the recess etch time. Atomic Force Microscopy was used to measure the width of the recess. We studied the effect of the gate recess width on the DC and microwave properties of 0.9 µm gate length transistors. The best performance was obtained for a recess etch time of 1 minute, resulting in a recess width of 0.22±0.05 µm. For this recess etch width, we measured a maximum drain current of 530 mA/mm, a transconductance of 320 mS/mm, f_T of 31 GHz, and f_{max} of 106 GHz.

INTRODUCTION

Pseudomorphic High Electron Mobility Transistors (PHEMTs) fabricated from InGaP/InGaAs layers on GaAs substrates have attracted attention as possible replacements for AlGaAs/InGaAs PHEMTs. Unlike AlGaAs/InGaAs devices, the InGaP/InGaAs PHEMTs do not suffer from DX center defects [1]. Higher breakdown voltages and improved power performance have been reported for InGaP/InGaAs PHEMTs [2]. A lower noise figure in InGaP/InGaAs PHEMTs compared to AlGaAs/InGaAs PHEMTs has also been demonstrated [3].

A key feature of the InGaP/InGaAs material system is the availability of highly selective etches. This is important for the manufacturability of PHEMTs, since a selective gate recess etch allows fabrication of devices with uniform and repeatable threshold voltages [4]. With a selective gate recess etch, the width of the recess trench can also be adjusted simply by changing the recess etch time. The width of the gate recess is a significant parameter in PHEMT structures [5].

In this work, we report a study of InGaP/InGaAs PHEMTs fabricated with gate recesses of varying width, obtained by selective wet etching. We compare the dc and microwave performance of the devices, and we measure the recess width with Atomic Force Microscopy (AFM).

DEVICE FABRICATION

We fabricated devices on an InGaP/InGaAs PHEMT epitaxial structure grown by MBE on a semi-insulating GaAs substrate. A schematic cross section of the device structure is shown in Figure 1. In the growth direction, the device structure consisted of a 5000 Å GaAs buffer layer, a 120 Å $In_{0.20}Ga_{0.80}As$ channel, a 10 Å GaAs smoothing layer, a 30 Å undoped $In_{0.49}Ga_{0.51}P$ spacer layer, a 30 Å $In_{0.49}Ga_{0.51}P$ donor layer Si-doped to $3x10^{19}$ cm^{-3}, a 120 Å undoped $In_{0.49}Ga_{0.51}P$ layer, and a 400 Å GaAs ohmic contact enhancement layer Si-doped to $5x10^{18}$ cm^{-3}. We etched off the top n+ GaAs layer to perform Hall effect measurements, and obtained $n_s=3.2x10^{12}$ cm^{-2} and $\mu=1690$ cm^2/Vs at 300K, and $n_s=3.6x10^{12}$ cm^{-2} and $\mu=2510$ cm^2/Vs at 77K.

We used conventional contact lithography, metal liftoff, and mesa isolation to fabricate PHEMTs. The source and drain ohmic contacts were formed by evaporating Ge/Au/Ni/Au (180Å/340Å/110Å/2000Å) and annealing for 30 s at 390°C in a rapid thermal annealer. Device isolation was obtained by mesa etching, using a series of selective wet etches. We etched the GaAs and InGaAs layers in H_3PO_4:H_2O_2:H_2O (3:1:50) at 19°C, and the InGaP layer in H_3PO_4:HCl (9:1) at 40°C. Just prior to the gate lithography, the wafer was cleaved into three parts which were given different recess etch treatments. The gate recess etch consisted of either 1, 2, or 4 minutes in a H_3PO_4:H_2O_2:H_2O (3:1:50) solution at 19°C. Following the gate recess etch, Ti/Au (1000Å/6000Å) gate metal was evaporated for liftoff.

RESULTS AND DISCUSSION

For each gate recess etch time, we determined the recess width, parasitic series resistance, threshold voltage, maximum drain current, transconductance, reverse breakdown voltage, f_T, and f_{max}. The results are summarized in Table 1. In the sections below, we describe the characterization procedures and discuss the results.

Recess Width Measurement

The width of the gate recess, L_R, was measured using an Autoprobe CP model Atomic Force Microscope (AFM) from Park Scientific Instruments. The AFM allows accurate measurements of the gate recess profile. We prepared a series of test structures with a gate recess process identical to the actual devices, but a thin (~400 Å) gate metallization to facilitate AFM probing. An example of an AFM image of the gate recess is shown in Figure 2. We defined L_R as the separation between the edge of the gate metal and the bottom of the etched n+ GaAs sidewall, as shown in Figure 1.

With the AFM, we were able to able to identify a non-uniformity in gate recess width at longer etch times. The values of L_R in Table 1 are median values, and the standard deviation in L_R increased from 0.05 µm for a 1 minute etch to 0.15 µm for a 2 minute etch and 0.23 µm for a 4 minute etch. On some of the test structures, the gates were offset to one side of the gate recess. We believe that this is due to the wafers being tilted slightly with respect to the flux in the evaporation chamber. For these wafers, we averaged the recess width on either side of the gate to obtain a value for L_R.

Series Resistances

The source and drain series resistances were measured with a Floating Gate Transmission Line Method (FGTLM) [6]. The total source to drain resistance was measured in a four probe configuration, with the gate floating. This measurement was repeated for devices with gate lengths ranging from 0.9 µm to 2.5 µm. The total resistance was plotted against gate length, and extrapolated linearly back to zero gate length to obtain R_s+R_d. We believe that R_s+R_d is a better indicator of series resistance in our devices than either R_s or R_d alone. Unless electron-beam lithography is used, misalignments of the gate mask level can result in the gate being offset towards either the source or drain. As noted above, slightly angled gate metal evaporation can result in the gate being offset to one side of the gate recess. These two effects change R_s and R_d, but we expect the sum R_s+R_d to be approximately independent of gate placement.

DC Characterization

On-wafer DC current-voltage measurements were made with an HP 4145 Semiconductor Parameter Analyzer. In Figures 3 and 4, we show typical device I-V curves for a 0.9 µm gate length PHEMT fabricated with a 1 minute recess etch. From the device I-V curves, we extracted the maximum drain current I_{dmax}, the peak transconductance g_m, and the threshold voltage V_{th} at V_{ds}=4V. We also measured the gate to drain reverse breakdown voltage (where $|I_g|$=1 mA/mm) with the source floating, and the gate to source reverse breakdown voltage with the drain floating. These two values were averaged to obtain a single reverse breakdown voltage, V_{bd}. In Table 1, we report mean values of I_{dmax}, g_m, V_{th}, and V_{bd} for about 5 devices for each gate recess etch time.

We found that as the gate recess etch time is increased, V_{th} becomes more positive, I_{dmax} and g_m both drop, and V_{bd} increases in magnitude. The change in V_{th} suggests that the InGaP barrier is being thinned slightly by the recess etch. From the shift in threshold voltage, we estimated the etch rate on the InGaP layer to be 14 Å/minute. The drop in I_{dmax} and g_m with increasing etch time is due to a combination of the increased source resistance and the slightly decreased gate to channel separation.

Microwave Characterization

On-wafer microwave measurements were made with an HP 8510 Network Analyzer. Scattering parameters were measured as a function of device bias at a frequency of 12 GHz. At the bias for peak current gain, we extrapolated the current gain $|H_{21}|^2$ and the unilateral gain U at -20 dB/decade to obtain f_T and f_{max}. The charging delay of the 28 fF gate contact pad capacitance was then de-embedded from f_T and f_{max}. We found that f_T and f_{max} both decreased with increasing recess width. The best microwave performance, with f_T of 31 GHz and f_{max} of 106 GHz, was obtained for a 0.9 µm gate length device with the shortest etch time, 1 minute.

A delay time analysis of the microwave data indicated that an increase in the drain delay with increasing recess width was partly responsible for the drop in performance. The drain delay was extracted from the variation in peak f_T with drain to source voltage, according to the procedure described in [7]. For the 1 minute etch, the drain delay was 0.12 ps, while for the 2 minute etch it was 0.70 ps.

SUMMARY

To investigate the effect of the gate recess width on PHEMT performance, we fabricated three sets of $In_{0.49}Ga_{0.51}P/In_{0.20}Ga_{0.80}As$ PHEMTs using a selective wet etch process for the gate recess. The transistors were identical except for the gate recess etch time. We used an Atomic Force Microscope to accurately measure the lateral profile of the gate recesses, and we estimated the extent of thinning of the InGaP barrier from a shift in threshold voltage with etch time. As the gate recess is widened, we found that the source and drain series resistances increase,

and the magnitude of the gate reverse breakdown voltage increases. Transconductance and maximum drain current both decrease with increasing recess etch time, due to a combination of the increased series resistance and the decreased gate to channel separation. Microwave measurements showed that f_{max} and f_T both decrease with increasing gate recess etch time. A delay time analysis attributed this partly to an increase in the drain delay.

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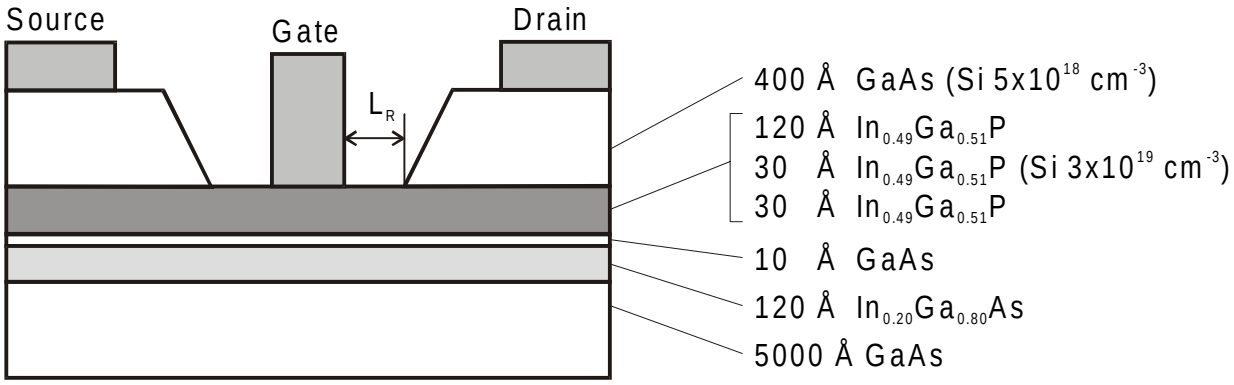

Figure 1. Cross section of recessed gate InGaP/InGaAs PHEMT structure. L_R is the gate recess width.

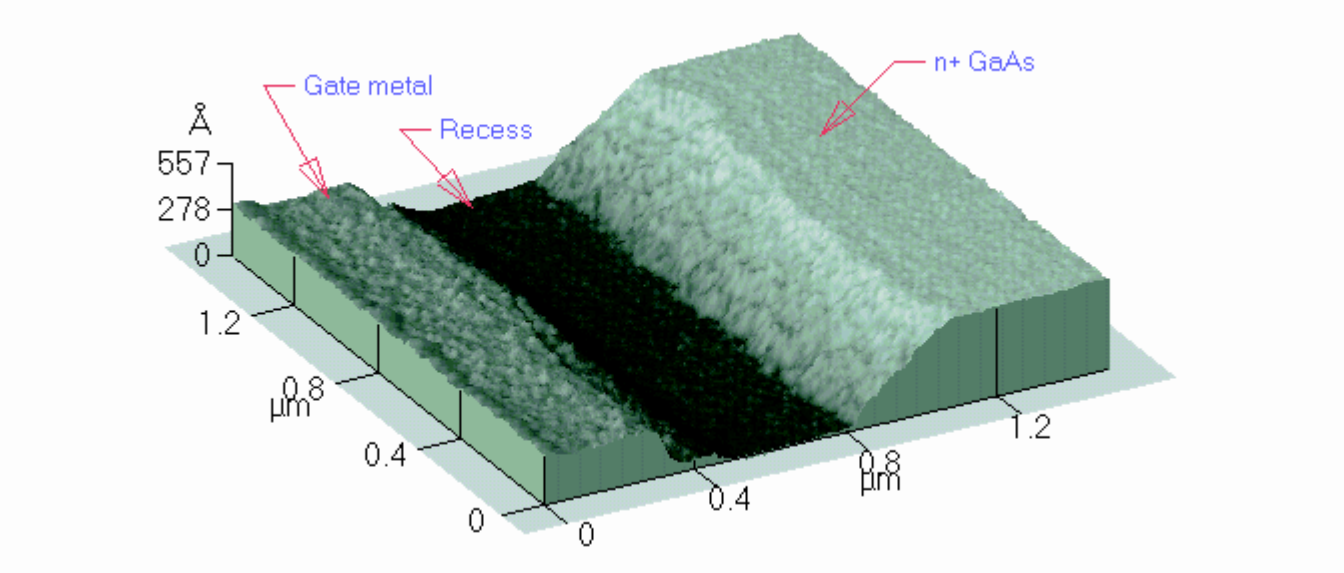

Figure 2. AFM image of gate recess fabricated with a selective wet etch process. The floor of the recess trench is InGaP, and the gate metal in this test structure is thin (~400 Å) to facilitate AFM probing.

TABLE I
CHARACTERISTICS OF 0.9 µm GATE LENGTH InGaP/InGaAs PHEMTS

Gate recess etch time, t_{etch}	1 minute	2 minutes	4 minutes
Recess width, L_R	0.22 µm	0.49 µm	0.89 µm
Threshold voltage, V_{th}	-0.90 V	-0.70 V	-0.40 V
Maximum drain current, I_{dmax} (at V_{ds}=4V)	530 mA/mm	510 mA/mm	260 mA/mm
Peak transconductance, g_m (at V_{ds}=4V)	320 mS/mm	300 mS/mm	220 mS/mm
Gate reverse breakdown voltage, V_{bd}	-6 V	-7 V	-12 V
Total series resistance, R_s+R_d	1.7 Ωmm	2.4 Ωmm	3.1 Ωmm
Unity current gain frequency, f_T	31 GHz	22 GHz	19 GHz
Maximum frequency of oscillation, f_{max}	106 GHz	80 GHz	62 GHz

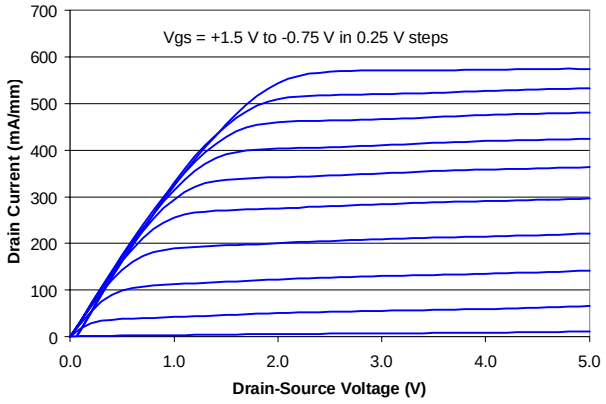

Figure 3. I_d-V_{ds} characteristics of 0.9 µm gate length InGaP/InGaAs PHEMT with 1 minute recess etch.

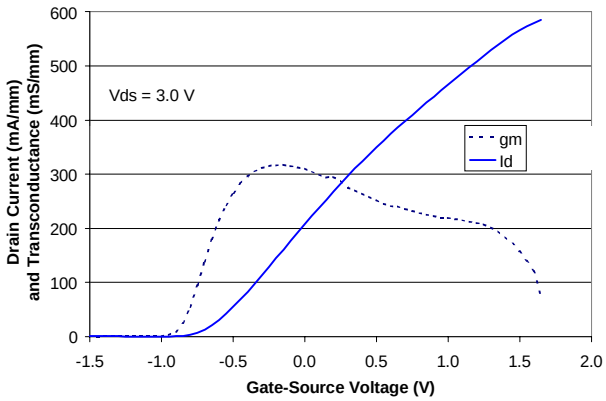

Figure 4. I_d-V_{gs} characteristics of 0.9 µm gate length InGaP/InGaAs PHEMT with 1 minute recess etch.