Economic Justification of a 6” GaAs Wafer Fab

Jerry Gedaly
Raytheon Company
Advanced Device Center
Andover, Massachusetts

ABSTRACT

The demand for high speed Gallium Arsenide (GaAs) products has increased such that the technology is expanding beyond niche markets and is entering commodity markets. The ultimate acceptance of GaAs in commercial applications, however, depends upon its providing the lowest cost solution compared to other technologies.

To achieve lowest manufacturing costs, many GaAs companies have embraced the “Silicon Model”, which continually increases wafer diameter. Over the last ten years, GaAs wafer sizes have increased at a rate equal to one-half the diameter of the typical silicon wafer. GaAs conversion to 6” is occurring simultaneously with Silicon conversion to 12” wafers.

Justification for conversion to a larger wafer size in a “moderate volume” GaAs fab is based upon economic arguments which consider Total Cost. To do this, the “arguments” are converted to algorithm-based cost models, which take into account existing conditions and predict future outcomes prior to expenditures.

The characteristics of the moderate volume Gallium Arsenide wafer fab include: low overall capital utilization, single points of failure, and low operator productivity. In spite of these disadvantages, the cost advantage of larger wafer sizes can be demonstrated. Modeling steers process, equipment, and staffing decisions that must be made to achieve optimal operating metrics.

INTRODUCTION

Economic justification begins by defining the elements of Total Cost. Four elements were identified; labor, capital (depreciation), overhead, and raw substrate. Labor includes operators, supervisors, engineers, and other support functions. Capital includes equipment and building. Overhead consists of supplies, repair materials, outside services, employee related expenses, occupancy expense (utilities, rent, facilities support), and allocation charges (management staff). Raw substrate is a separate element to highlight the cost differences between implanted versus epitaxial (MBE, MOCVD) substrates.

The next step is to accurately calculate how these cost elements scale between 4” and 6” wafer sizes. Area comparison (using the ratio of the wafer radius squared) is 2.25X more area on a 6” wafer as compared to a 4” wafer. As expected, most cost elements scale favorably, but not all.

Once the cost differences are determined, the cost elements are normalized to unit area to facilitate die cost comparison. The unit “cost per millimeter squared” is suggested. For this presentation, however, comparisons will be proportioned to 1 (100%).

DISCUSSION

A wafer cost model has been created in EXCEL that contains the four elements of total cost versus increasing wafer volume. It contains algorithms that were built based upon experience as well as benchmarks obtained from other GaAs wafer fabs. The following volume driven algorithms are included in the cost model:

Line yield
Operator productivity
Support staffing
Supplies
Repair materials
Depreciation
Raw wafer cost

Element 1: Operator labor cost has three components, each easily measured; productivity (moves per labor hour), line yield (how many moves to make an out), and wage rate. Productivity difference between 4” and 6” was calculated by comparing the equipment set on the existing 4” line with the recommended equipment for the 6” line. Platen or planetary based tools scaled unfavorably. Many single wafer tools compared quite favorably, and lithography tools broke even. Overall, productivity is expected to decrease (per wafer) by 20%, yet increase (per unit area) by 50-75%. A list of the key tools and their scaling efficiencies are shown in Fig. 1.

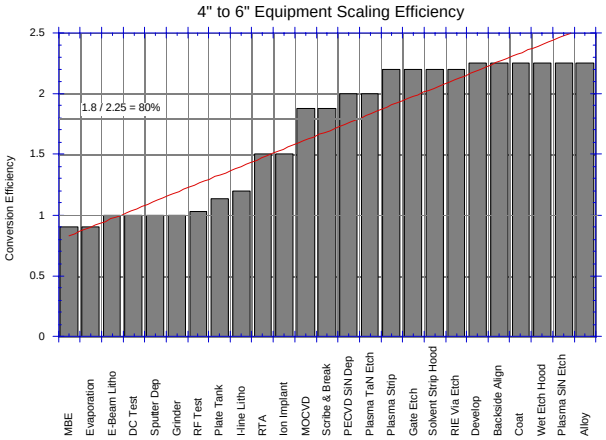

Fig.1 - Equipment Scaling Efficiency

The second component, line yield, trades-off increased breakage due to handling a larger wafer and reduced breakage due to increased automation (cassette to cassette handling). Also, yield was reduced by expected parametric loss due to poorer uniformity of the larger 6" wafer, yet increased by the improved process capability of the advanced 6" tools. The model assumed a line yield decrease by 7% for the 6" line versus the 4" line. Wage rate was held constant. Support labor was expected to increase (per wafer) by 20%. Resultant Total Labor Cost per Wafer is shown in Fig. 2.

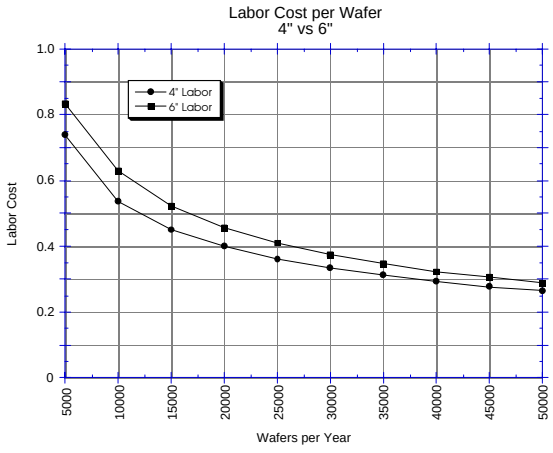

Fig. 2 - Total Labor Cost

Element 2: Capital costs are shown as depreciation based on accounting methods used by Raytheon. A capacity model was created in EXCEL to determine the equipment requirements versus increasing wafer volume. This model created the volume driven depreciation algorithm. Its components were:

- Process flows (MESFET, PHEMT, HBT)
- Operation yield
- Run rates and Batch sizes per tool
- Uptime
- Work schedule
- Mix

Utilization % for full capacity can be selected based upon planned cycle time and variability. The depreciation algorithm has a fixed component, which is equivalent to the first year depreciation on the capital required to run one wafer, and a variable component, which is predicted by the model. Figs. 3 and 4 show equipment utilization profiles for pilot and moderate volume production.

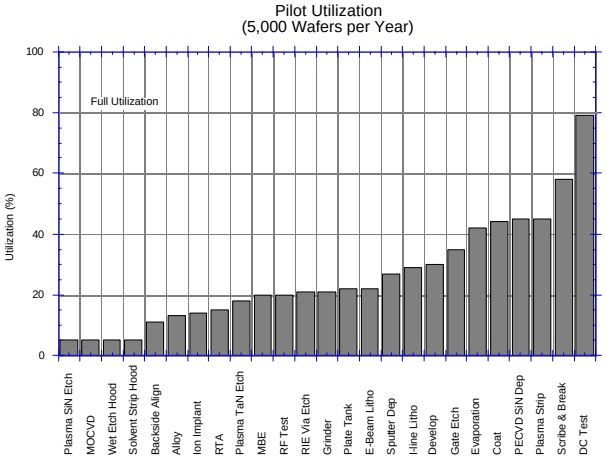

Fig. 3 - Equipment Utilization of a Pilot Wafer Fab

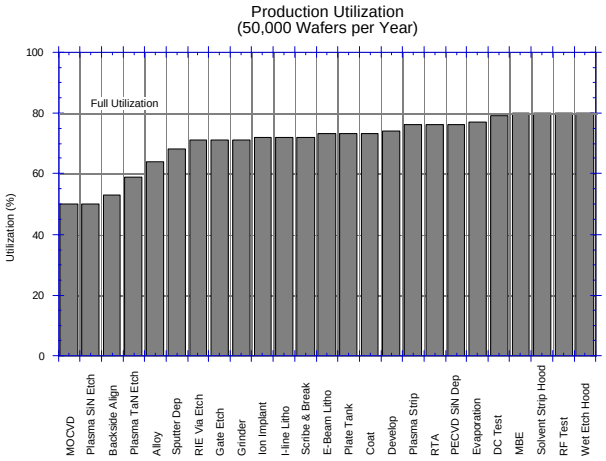

Fig. 4 - Equipment Utilization of a Production Wafer Fab

Once all of the tools on the "pilot" line are fully utilized, capital costs become linear with increasing volume (Fig. 5). The depreciation (per wafer) is higher on the 6" line, a result of purchasing tool automation and process capability.

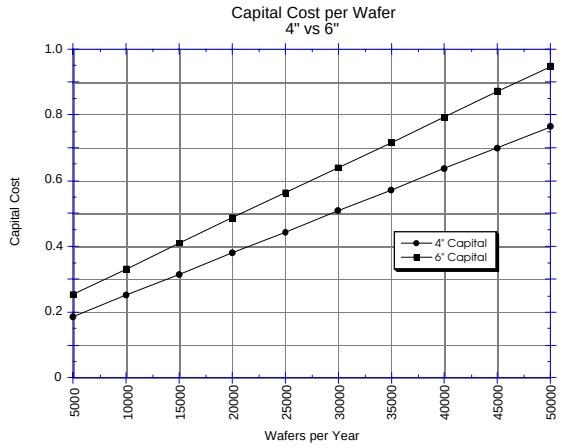

Fig. 5 - Capital Cost for 4" and 6" Wafer Fabs

Element 3: Overhead consists of supplies, repair materials, outside services, employee related expenses, occupancy expense (utilities, rent, facilities support), and allocation charges (management staff). Fig 6 shows the main categories; how they scale versus volume, and how they compare by wafer size. Variable cost portion of supplies scale by 1.5X. Repair materials scale by 1.2X. Allocation and occupancy are identical, but are charged based upon headcount and square footage, respectively.

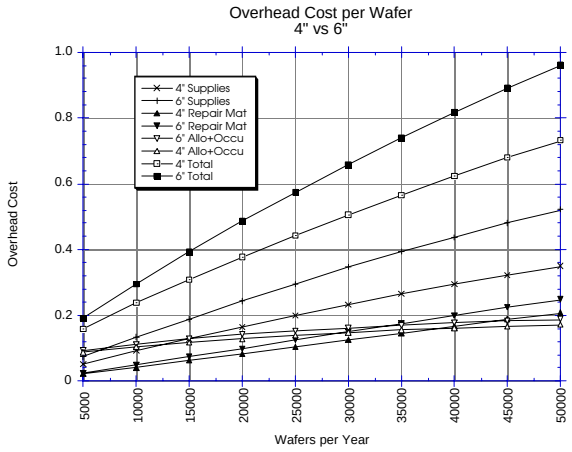

Fig. 6 - Components of Total Overhead Cost

Element 4: The source wafer for MESFET is assumed to be an unimplanted GaAs wafer. The source wafer for PHEMT and HBT are assumed to be MBE and MOCVD respectively. Raw wafer cost is expected to scale as shown in Table 1. Wafer prep (implant and anneal) for the MESFET source wafer is considered separately.

TABLE I
RAW WAFER SCALING FACTOR

Substrate Type	6"/4" Cost	Explanation
GaAs	2.25X	Raw material dominates cost
MBE	2.25X	Platen based reactor design
MOCVD	1.5X	Vertical tube reactor design

CONCLUSION

The results of the analysis is depicted in Fig. 7. Total cost for 4" and 6" wafers for three different processes (MESFET, PHEMT, HBT) are plotted. On a per wafer basis, the improvements for MESFET, PHEMT, and HBT are 42%, 30%, and 38% respectively.

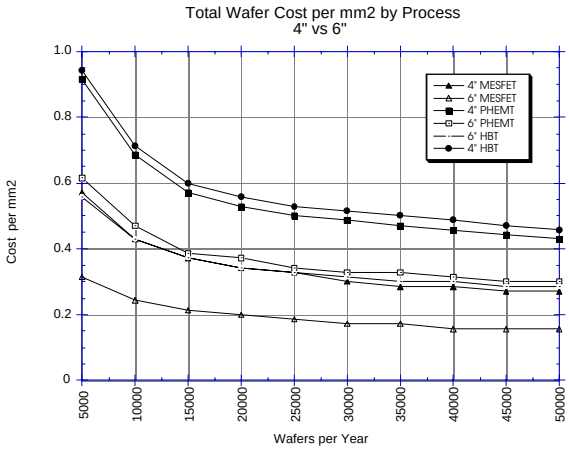

Fig. 7 - Total Cost per Wafer

In the case of a moderately loaded wafer fab, a more accurate way to compare costs is on a unit area basis. For example, a conmpany with a demand of 50K 4" wafers per year would have to run only 22K 6" wafers to make the same output. Figure 8 shows the result of comparing total cost on unit area basis. On a unit area basis, the

improvements for MESFET, PHEMT, and HBT are 30%, 18%, and 25% respectively.

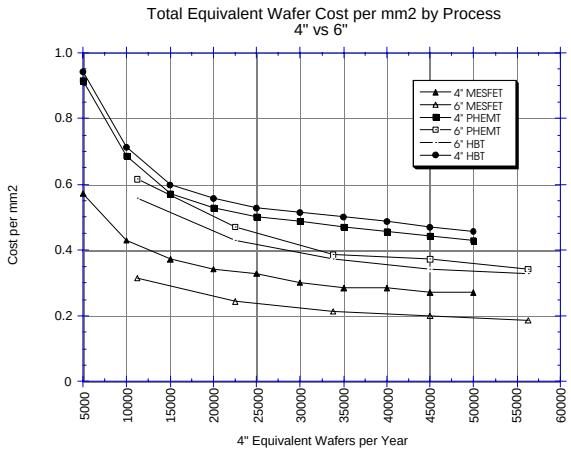

Fig. 8 - Total Cost per Unit Area

The cost components at moderate volumes (25K per year) for the each process, 4" and 6", are represented in Fig 9. As expected, MESFET has the lowest raw wafer component. However, in all three processes, substrate becomes a larger component at larger wafer size. This is because raw wafer scales least favorably. Conversely, labor becomes a smaller component for all three processes at larger wafer size. Other conclusions are less obvious.

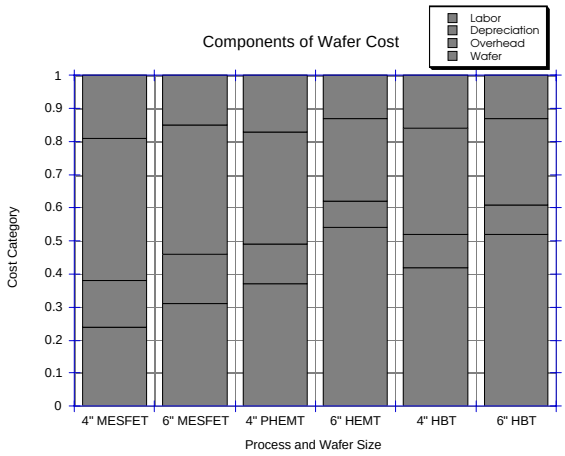

Fig. 9 - Total Cost Breakout

To conclude, total wafer cost for three different processes were determined for 4" and 6" substrates. The cost advantage of the larger wafer size held across all processes. Labor, depreciation, and overhead were slightly higher on a by wafer basis, but significantly lower on an area basis. Raw wafer costs differed by process, and MOCVD scaled slightly better than MBE.