# Process Simulation and Fabrication of Power Heterojunction Bipolar Transistors

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**ABSTRACT**

**Heterojunction Bipolar Transistors (HBTs) are considered excellent candidates for low phase noise millimeter wave applications. They exhibit outstanding high frequency performance and also low baseband noise compared to MESFET and HEMT devices. We have designed and demonstrated state-of-the art microwave and millimeter wave power HBTs using the baseline HBT process at HRL Laboratories. An HBT that is capable of delivering hundreds of mW of power across a broad frequency range has been developed. This paper presents process simulation and preliminary results on the fabricated multifinger power HBT devices.**

## INTRODUCTION

The development of InP power Heterojunction Bipolar Transistors (HBTs) has enabled high performance microwave and millimeter wave circuits. Indium Phosphide HBTs exhibit superior 1/f noise and high linearity compared to their HEMT counterparts. In this research effort, we demonstrated multifinger HBTs for microwave and millimeter wave applications.

Circuit designs that require large current drive often use multiple discrete devices in parallel to deliver the output power needed. Since this technique consumes excessive die area, an alternative layout scheme with a smaller footprint is desirable. Many publications have shown the effectiveness of multi-emitter-finger HBT devices and have addressed the issues concerning breakdown when one finger of the device consumes the majority of the current [1-4]. The corrective action of adding ballasting resistors is also discussed in the literature.

The goal of this work is to produce multi-finger devices capable of delivering hundreds of milliwatts of power that can be fabricated in-line with the baseline devices without additional epitaxial or thin film layers. The power HBT devices discussed in this paper were integrated into the baseline HBT process to provide output power capabilities not available in the current process and set of design rules. The epitaxial layer structure of these power devices is identical to that of the baseline devices. The larger power devices fabricated here are HBT transistors with multiple emitter fingers ranging from 4 to 12 fingers. The individual emitter fingers for the various devices utilized $2x5\mu m^2$ emitter metal structures.

In terms of minimizing the die area for these devices, the optimal layout would consist of unit cell transistors connected immediately adjacent to each other with no spacing between the cells. Several issues arise in building multi-finger power transistors by simply adjoining the unit transistor cells into a large device. The proximity of the adjacent feature is a concern with respect to intermetal dielectric film thickness the details of which will be discussed in the following section.

## PROCESS SIMULATIONS

Several issues exist in applying commercially available process simulation tools, which were designed for silicon integrated circuits (ICs), to the fabrication of III-V-based devices. For this reason process simulations are not widely used to date in the compound semiconductor industry. These issues arise from the inherent differences in the fabrication techniques used in the separate device technologies.

Recently, computer simulations were applied to model HBT fabrication at HRL Laboratories, LLC. (HRL) [5,6]. The simulation tools used in this work were commercially available Technology Computer Aided Design (TCAD) software packages designed to simulate silicon integrated circuit fabrication [7,8]. The HBT fabrication process at HRL involves mesa-isolating the devices and uses polyimide as the intermetal dielectric. Polyimide is spun on and then etched back to expose the emitter metal pattern of the device. Via holes are then etched into the polyimide to make contact to the base and collector metal patterns.

Process simulations were conducted in the work described here to analyze the feasibility of manufacturing multiple finger devices consisting of the basic HBT unit cell from the CAD library. The ultimate goal was to develop a basic set of design rules for fabricating these devices.

Accurately simulating the profiles of the spun-on inter-metal dielectric films over extremely non-planar surfaces is a challenging task for silicon-based TCAD software. The proximity of adjacent features, such as the various mesa structures in the proposed device designs, affects both the planarity of the dielectric films as well as the

ultimate film thickness over the different device types. It is known that devices with larger surface areas result in thicker dielectric films. Process simulations were used to evaluate several proposed device configurations. Further simulations developed a process flow and layout rules for the mesa spacing in the multi-finger devices. One major goal of the TCAD simulations was to develop a process flow that could be utilized to fabricate both power and baseline devices monolithically.

Process simulations were used to analyze the polyimide thickness over the various proposed device layouts. Initial simulations characterized the polyimide film thickness over the standard devices following the baseline design rules. The simulated thickness over each mesa level (emitter, base, collector, and field) was calibrated using SEM cross-sections of existing baseline devices. The TCAD tools used in this work simulated the profiles of spun-on films by convolution of the initial device profiles with a Gaussian function. Once the planarizing properties of the polyimide film were characterized, it was possible to simulate profiles on any arbitrary device or circuit layout. Further simulations confirmed the fact that it was possible to adjoin unit HBT cells with no spacing. That is to say that the polyimide thickness over these larger devices, while indeed thicker than over the baseline devices, was still within the process window of the etch-back process used to expose the emitter metal patterns.

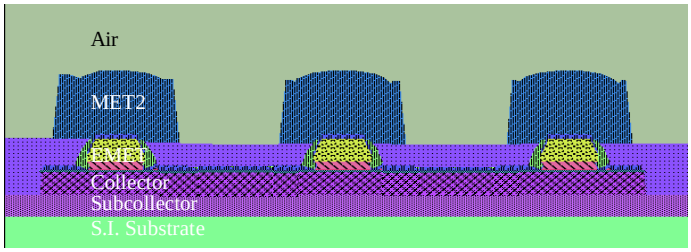
## DEVICE CROSS-SECTIONS

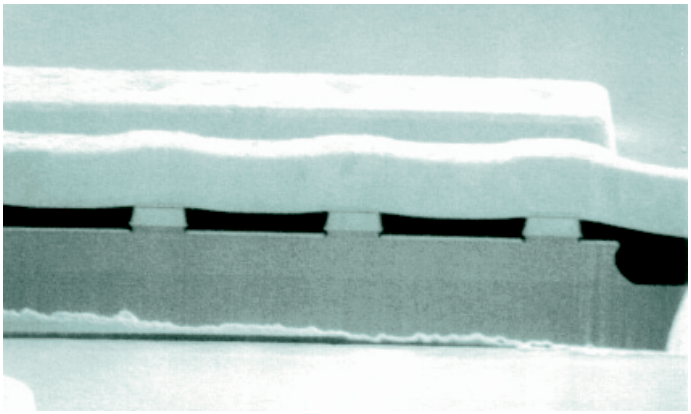
After confirming the feasibility of joining unit cells, two basic device layouts were considered. The first type of devices is formed with a continuous base-collector mesa (figure 1). The second type of device utilized separate base-collector mesas for each individual emitter finger (figure 2). The multi-finger HBT devices were fabricated using the "baseline" HBT process flow at HRL. The fabrication of these transistors resulted in device yields that were consistent with the yields of the baseline devices.

Figures 1 and 2 show simulated cross-sections along with Focused Ion Beam (FIB) cross-sections for comparison. The simulated cross-sections for both types of devices show excellent agreement with the fabricated devices. Although the polyimide is thicker over the emitter metal patterns in the power devices, sufficient process latitude exists to fabricate both devices monolithically using the baseline process flow.

The transistor shown in figure 2 is an example of a device that was intentionally biased into breakdown to investigate the failure mechanism. Breakdown occurred here in a single finger as a result of "current hogging" [1]. The devices suffered the expected catastrophic avalanche breakdown as in the baseline devices. No

(a)

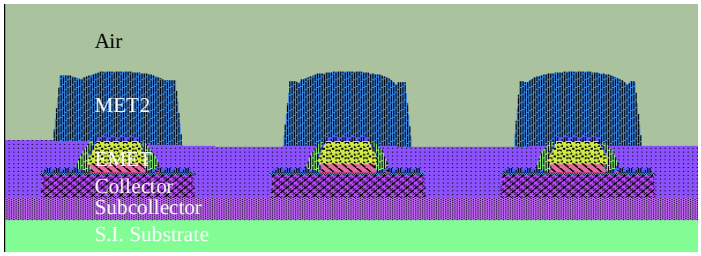


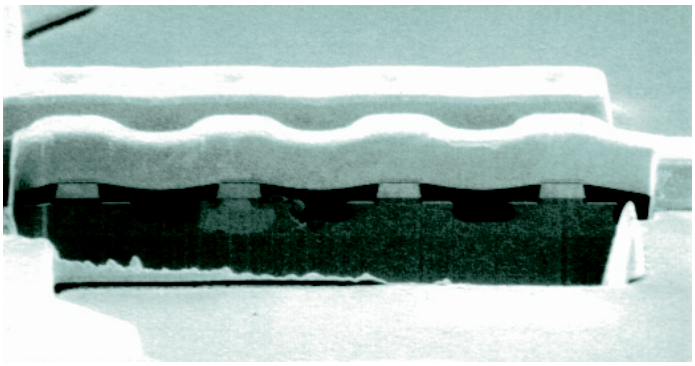
(b)

Figure 1

Simulated cross-sections of a Power HBT device illustrating the configuration with a continuous base-collector mesas. Figure (a) shows the simulated cross section. Figure (b) shows a fabricated device that has been prepared for cross-sectional viewing by FIB milling.




(a)



(b)

Figure 2

Simulated cross-sections of a 5-finger Power HBT device. Both figures show the configuration with separate base-collector mesas. Figure (a) shows the simulated cross section. Figure (b) shows a fabricated device that has been prepared for cross-sectional viewing by FIB milling.

secondary mechanisms were observed which lead to an artificially low breakdown. Prior to fabrication, it was thought that the devices with separate mesas would suffer from early breakdown due to the high field present at the base-collector junction of each device finger.

Process simulations were used successfully here to develop layout rules and a process flow *a-priori* for fabricating power HBT devices monolithically with standard switching transistors. These simulations lead to first-pass success which equates to a savings of time and money.

Figure 3 below is an optical micrograph of a five-finger power HBT with separate base-collector mesas. The individual mesas are visible in the photo. The nomenclature 25B5FNC in this figure refers to the use of the standard 2x5$\mu m^2$ emitter pattern with 5 fingers and the base-collector mesas are not connected. This figure illustrates the minimum die area of these power devices.

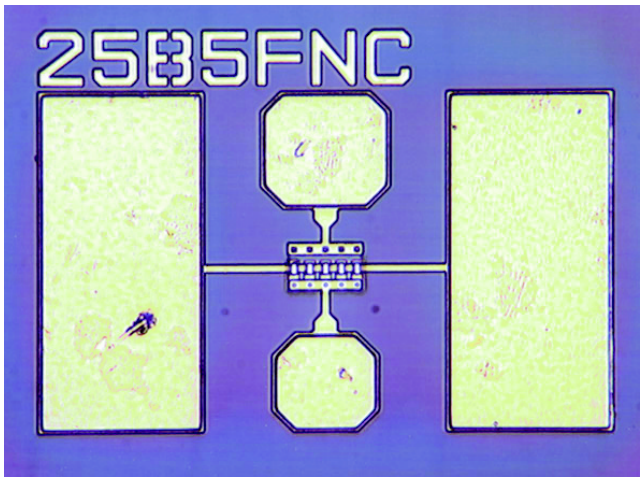



Figure 3
Optical Photograph of five-finger power HBT device
with separate base-collector mesas.

## DC DEVICE CHARACTERISTICS

A forward Gummel plot of a 12-finger device with a continuous base-collector mesa is shown in figure 4. The maximum DC current gain (beta) was 50 for this device at a current density of $J_c = 1.7*10^5$ A/cm$^2$.

Figure 5 shows the $I_c$-$V_{ce}$ characteristics of the same device. From this figure it can be seen that the device is capable of delivering a minimum of 400mW of power. The $I_c$-$V_{ce}$ data in figure 5 also shows little evidence of avalanche breakdown at these bias conditions.

## CAPACITANCE EXTRACTION

DC voltage sweeps were performed on each junction (base-emitter and base-collector) individually while shorting the other junction. The Levenberg-Marquart [9]

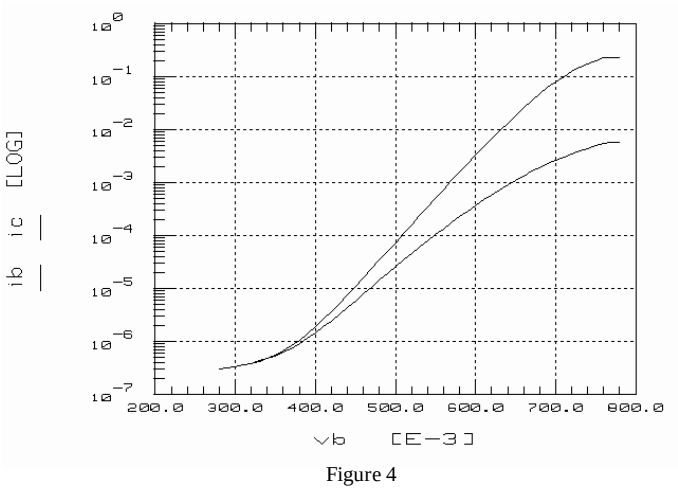



Figure 4
Forward Gummel curves of a 12-finger power HBT
device with separate base-collector mesas.

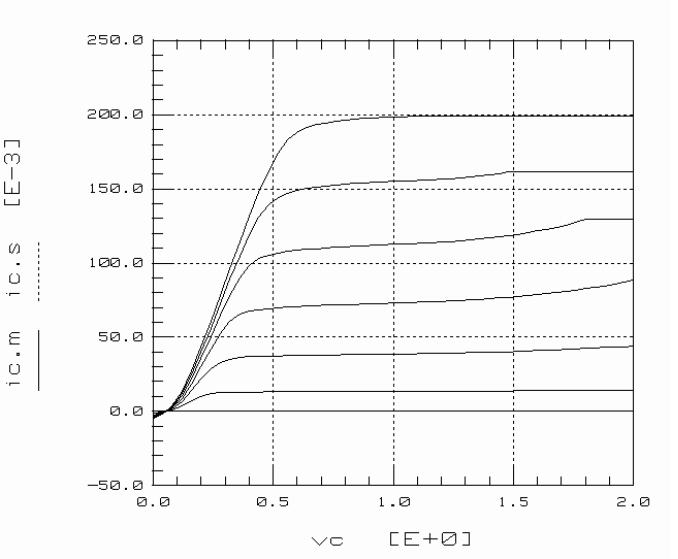



Figure 5
DC $I_c$-$V_{ce}$ curves of a three-finger power HBT device.

algorithm was then used to optimize the values of the junction capacitance terms using the measured y-parameters. The terms used in the optimization were $C_0$, $\phi$, and M, using the equation:

$$C(V)=C_0*(1-^V/_\phi)^{-M} \qquad [10]$$

where $C_0$ is the zero bias junction capacitance, $\phi$ is the built-in potential and M is the power dependence of the depletion width. Typically the value of M is 0.5 for homojunctions and around 0.3 for heterojunctions.

Figure 6 plots the junction capacitance terms, $C_{je0}$ and $C_{jc0}$, extracted for each style of multi-finger transistors. The figure shows that the devices with more fingers exhibit larger capacitance at both junctions as was expected. The data shows little variation in base-emitter

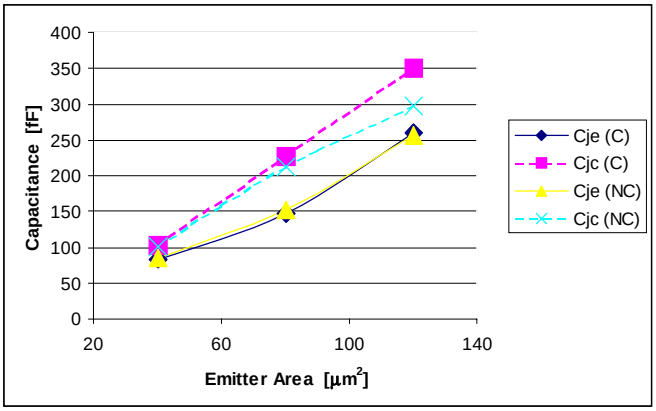



Figure 6
Capacitance values of the multifinger devices prepared in this work. The labeling C and NC in the legend specify whether the base-collector mesas were connected (C) or not connected (NC).

junction capacitance ($C_{je}$) between the devices with and without a continuous base-collector mesa. This is due to the fact that the emitter-base junction area is determined solely by the emitter metal pattern in our self-aligned mesa fabricated devices.

A distinct difference is noticed, however, in the junction capacitance at the base-collector junction ($C_{jc}$) between device styles. The additional junction area that exists between the emitter fingers in the connected-mesa transistors explains the larger $C_{jc}$ values for these devices.

## CONCLUSION

Using process simulation tools, we have developed a set of design rules and a process flow for fabricating multiple-finger HBT devices capable of delivering hundreds of milliwatts of power. Process simulations were used in this case to insure at first-pass success and to develop a set of design rules that consume the minimum amount of die area. These power HBT devices are fabricated in-line with the baseline HBTs that are produced at HRL. These new multiple finger transistors allow our designers a new level of flexibility in circuit layout. The smaller footprint of these devices also serves to increase circuit yield compared to designs that utilize large numbers of transistors in parallel to achieve the desired current drive.

The devices and design rules developed in this work resulted in a 40% reduction in the die area required to achieve the same total output power. This figure is based upon using 8 discrete transistors following the baseline design rules compared to a single 8-finger device.

## ACKNOWLEDGEMENTS

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