

Heterostructure Device Wafer Manufacturing for Telecom Applications for 4" and 6" Wafer Fabs

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ABSTRACT

Epitaxial device wafers are becoming increasingly important for microwave, wireless and telecom circuits. Currently, 4" wafers can be controllably produced in volume, and there is a movement towards 6" wafers. The primary motivation to migrate towards 6" fabrication is the cost advantages which can increase market penetration of GaAs based circuits. Successful manufacturing of 6" epitaxial wafers critically depends upon the availability of high quality substrates and epitaxial growth technology to produce thin, highly uniform layers over large areas. In addition, vigorous statistical process control of the epitaxial growth process is essential for high volume manufacturing of heterostructure devices. Preliminary results indicating good heterostructure layer characteristics demonstrate the feasibility of 6" AlGaAs-based HBT device wafers. Specific features of the HBT structure and manufacturing process may facilitate this technology's transition to 6" wafers.

INTRODUCTION

The wireless industry continues its double-digit growth driven in large part by cell phone systems and specifically handset sales. Estimates show the handset market doubling every two to three years with projections for 200 million digital units sold annually by the year 2000. Equally impressive growth is taking place in the optical communications markets. Popular estimates are for a 25x increase in bandwidth between 1995 and 2005. The need for more bandwidth for telecom and datacom traffic increases demands for higher frequency wavelength division multiplexing (WDM) SONET/SDH and ATM systems and in turn, chipsets at 2.5, 10 and 40 Gb/sec data rates.

As communications markets evolve, insatiable consumer demand for leading edge product features create opportunities for enabling technologies. Products with superior performance, portability, and lower cost need to be continually brought to market. One of the best examples of an enabling epitaxial structure and process technology in recent times has been the GaAs

heterojunction bipolar transistor (HBT) circuit. The HBT circuit market has grown in three short years from several million dollars annually to over \$250 million. Projections are for a doubling of the market over the next two years. This rapid technology adoption and substantial projected growth rate are directly related to the cost effective system solution HBTs provide to the users.

A "BUILT-IN" EPITAXIAL DEVICE SOLUTION

A new paradigm has arrived for circuit manufacturers, currently for telecom circuits but for broader applications at later stages. Unlike traditional circuit manufacturing where the devices are create in the wafer fabs, HBT wafer providers deliver wafers with fully-grown transistors, hence the reference to these as *device wafers*. The HBT is a vertical transistor with electron transport from top (the emitter) to bottom (the collector). DC and RF properties are determined by the vertical dimensions of the transistor and controlled by the epitaxial growth process. The epitaxial growth process and equipment must be capable of controlling atomic layer thicknesses accurately, uniformly and reproducibly. This vertical transistor structure is very powerful, allowing high frequency, efficiency and linear performance, and is not constrained by the lithography limits which currently control the transistor performance of conventional horizontal field effect transistors (FET). Furthermore, the relaxation of lithography - - HBT circuit manufacturers use 1 to 2 μm design rules to delineate and connect the vertical HBT transistors - - results in higher circuit yields, and lower facilities and equipment costs, while still enjoying smaller die size owing to the 3-D nature of the transistors. In addition, the ability to design the HBT device structure using a variety of alloy compounds and multiple heterojunctions allows further performance improvements, and ease of fabrication. In fact, "application specific" and "process specific" transistor structures are now being developed and manufactured. HBT wafers present great challenges to the provider, but offers great value to circuit manufacturers.

The above mentioned performance advantages compliment the HBT's system benefits of single supply operation and the ability to completely turn-off, thereby

reducing battery drain without the need of an external drain switch component. Still, it took a long time for circuit and handset manufacturers to adopt HBT technology; the two main barriers to entry having been device reliability and the quality of the HBT wafers. The present commercial success of HBT circuits clearly indicate that these two barriers have been overcome. Device reliability is dependent upon circuit processing techniques and device layout, as well as epitaxial wafer structures and growth. Much effort has been spent over the years addressing reliability issues, and HBT devices and circuits have demonstrated outstanding reliability performance [1-2].

Let us now review the production of consistent HBT wafers and its implications regarding the migrating to 6" heterostructure circuit manufacturing.

HETEROSTRUCTURE WAFER PRODUCTION

As we have stated above, the critical device parameters are incorporated within the epitaxial layers. By the time the HBT circuit manufacturers receive the HBT device wafers, the vertical transistors are already grown resulting in arrays of vertical transistors for the wafer fab to "connect". HBT wafers, in many ways, present the most challenge to the wafer providers. Though epitaxial wafers are also grown for pseudomorphic high electron mobility transistors (PHEMT) structures used for microwave and telecom circuits, the final transistor characteristics in PHEMTs are determined by the process (gate recess, etc.) usually done by the circuit manufacturers. For HBTs, the transistor's characteristics are determined by the epitaxial growth process. The growth process must be able to accurately calibrate and control doping levels and thickness (resistivity), alloy compositions, interfaces, and junction formations. The finished device must exhibit very tight control and reproducibility of transistor parameters such as turn-on voltage (V_{be}), gain, base/collector breakdown voltage (BV_{cbo}), base sheet resistivity, emitter resistance, etc. The circuit manufacturers require wafers with excellent uniformity and reproducibility, within-wafer, wafer-to-wafer, and lot-to-lot. Without this, HBT circuit manufacturers cannot exploit the technical benefits (high performance and reliability) nor the economic benefits

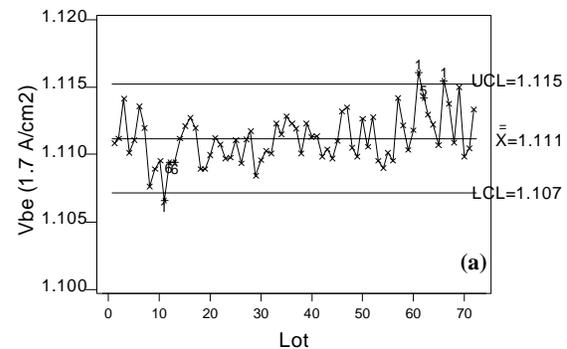
Device Parameter	Corresponding Layer(s)
Beta	base layer resistivity
V_{be}	p/n junction position
BV_{cbo}	collector layer
Emitter Resistance	hetero-interface transitions
Base Layer Resistivity	doping and thickness
Offset Voltage	junction characteristics

Table 1. HBT device parameters, and the related layer and interface parameters influencing the final device characteristic

(high yield and associated large die count per wafer) of HBTs. There are many interlocking parameters that have to be considered. Table 1 lists some of the device parameters and corresponding layer properties.

The wafer providers' systems must incorporate rigorous statistical process controls for effective volume production. Accordingly, the growth reactors must be carefully designed and maintained by a multidisciplinary technical team who fully understands Statistical Process Control (SPC). Calibration and testing procedures must be designed to assure all variables are well controlled. Additional testing is also necessary in process as well as post process to assure tight control of device parameters. The enormous range of these tasks is compounded by the fact that HBT vertical devices have different device structures, tailored for application-specific users and distinct fab processes. Therefore, thorough technical understanding and knowledge in device physics and growth processes are essential, and strengthen insights that can only be obtained from working with large sample sizes of diverse and varied layer combinations and interfaces.

SPC must be placed on key device characteristics to ensure device reproducibility. The following charts represent a particular product series of more than 6500 4" wafers. The transistor's V_{be} and base layer sheet resistivity are displayed in Fig. 1 and Fig. 2.



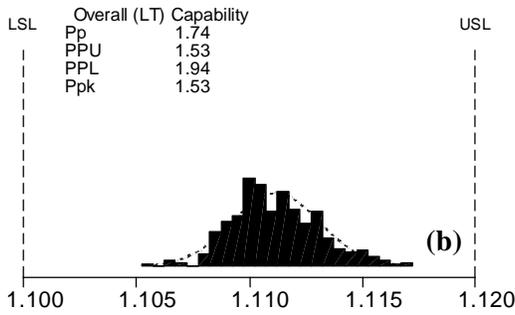


Fig.1 (a) SPC control chart for V_{be} incorporating the eight Standard Tests for special causes. Fig.1 (b) shows the corresponding capability chart. Statistical process control is demonstrated in Fig. 1(a) with the eight Standard SPC Rules applied. Fig. 1 (b) shows this process is capable with a capability index (P_{pk}) of 1.53. Likewise Fig. 2 shows the equivalent data for base sheet resistivity with a P_{pk} of 1.19.

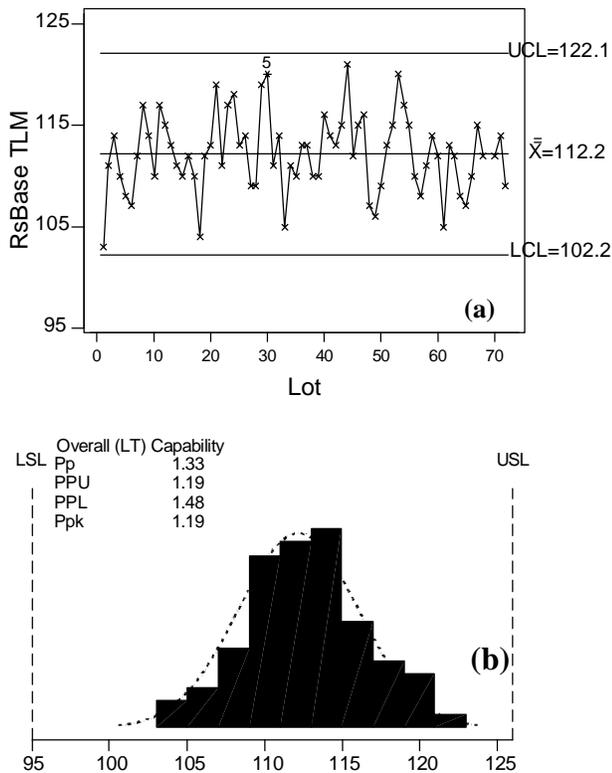


Fig.2 (a) SPC control chart for transistor base layer sheet resistivity. Fig. 2 (b) shows capability for this parameter.

Similar controls are also attained for other device parameters such as breakdown voltages, etc. Such vigorous control under real world manufacturing conditions has routinely allowed circuit manufacturers 95% end-to-end circuit yields.

Therefore, based on our own experience, and the fact HBT circuit manufacturers are having excellent commercial success, we can conclude that production of 4" HBT epitaxial device wafers have uniformity, reproducibility and reliability necessary for high volume commercial circuits. The versatile nature of HBT structures will continue to lead to new improved structures and future refinements, in performance, manufacturability and enhanced reliability. Epitaxial device wafers clearly have achieved the criteria necessary for repeatable performance, yield and volume throughput.

MIGRATION TO 6" PRODUCTION

The new challenge to wafer providers is the migration from 4" to 6" diameter wafers. The main driver for this migration is cost as the 4" to 6" transition promises approximately a 40% to 50% reduction in circuit processing costs. There may also be a per-unit-area savings in epitaxial wafer costs when multiwafer growth equipment is developed having the uniformity and reproducibility that HBT layers require. Circuit testing and packaging savings will be minimal. The circuit processing equipment costs will correspondingly increase when 6" equipment is used. Nevertheless, transition from 4" to 6" should lower the overall circuit costs. Furthermore, as circuits get more complex, chip sizes get larger having more transistors per circuit. A wafer with a 6" diameter would allow many more dies per wafer. Also, if device wafer providers can maintain the epitaxial wafer properties the same as those in 4", correspondingly high circuit yields are expected when combined with the relaxed requirements on circuit processing in HBTs.

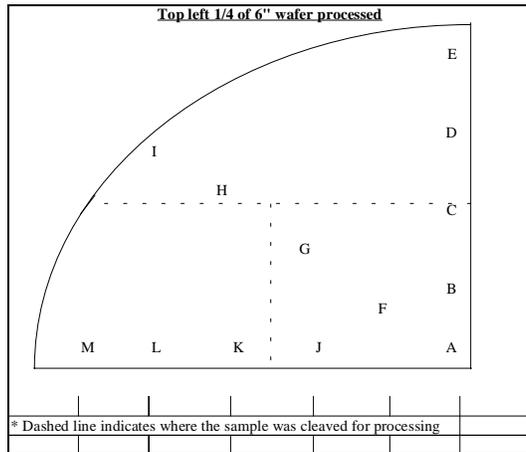
Interestingly, the situation is somewhat different in larger diameter PHEMT wafers. Specifically, the challenges in PHEMT migration include reproducibility in the threshold voltage, sheet channel charge, transconductance, and buffer layer characteristics. Layer uniformity will address some of these issues; sheet channel charge and buffer layer characteristics. The most challenging parameter will likely be threshold voltage, which unlike the turn-on voltage of HBT, varies as the square of layer thickness. Epitaxy offers a means to address this challenge with selective etch layers. In the case of PHEMT, InGaP alloys are being used not only as selective etch stop layers but also performance improvement mechanisms. InGaP enables higher breakdown, and potentially more reliable PHEMT devices.

A closer look at the challenges for 6" wafers reveals an interesting contrast in device technology. While the

conventional FET based solutions will rely heavily on the wafer fab's ability to scale processing steps (etching, implant, metalization), no such reliance is necessary for HBTs. In other words, transistor characteristics of a conventional FET can vary with transistor and processing scaling, while the intrinsic properties of HBTs should enable the 6" transition with a minimum of effort to the wafer fab and result in correspondingly high fab yields.

What are the main challenges to go from the current 4" to 6" epitaxial wafers? The main challenge is the epitaxial equipment and growth process. To maintain cost advantages, the growth chambers should be larger than currently used, resulting in uncertainties in uniformity, reproducibility, growth yields, etc. The wafer providers must translate their knowledge in equipment, growth processes, testing and other subtle features to the larger wafers. Though it is not an easy task by any means, it is our assessment that the technology has reached the maturity such that the transition is now possible.

Both molecular beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD) have been successful in providing excellent 4" device wafers, and both growth techniques are expected to provide 6" wafers also. In fact, since the MBE technique initially allowed growth equipment designs for accurate control of layer thicknesses, MBE techniques were favored in the early phase of device wafer production. However, the MOCVD technique has recently advanced greatly, such that very



Data Point	$\beta@1.7kA/cm^2$	$V_{be}@1.7A/cm^2$	BV_{cho}
A	24	1.1050	28
B	25	1.1046	28
C	26	1.1037	26
D	23	1.1050	29
E	34	1.1030	28
F	25	1.1041	27
G	25	1.1038	28
H	25	1.1036	28
I	35	1.0998	25
J	26	1.1037	28
K	27	1.1038	29
L	25	1.1046	28
M	36	1.1020	29
Mean	27.4	1.104	27.8
Std. Dev.	4.5	0.0014	1.2

Fig. 3. Large area device characteristics (L = 75 um x 75um) taken on a 1/4 piece of a 6" GaAs HBT device wafer. DC current gain, Vbe, and base collector breakdown voltage are shown in the table.

accurate control of layer properties is achieved. With its inherent flexibility of growing multiple alloys and compositions (such as InGaP), excellent wafer surface morphology, higher throughput advantage and ease of scalability both in equipment and growth processes to larger area growth, the MOCVD technique now enjoys a significant edge for volume production of device wafers.

We have been developing MOCVD 6" HBT device wafers and initial results are promising. Figure 3 shows uniformity of key device parameters in 6" wafers. Edge effects as well as minor amounts of substrate slip still need to be addressed. The other challenge is the availability of high quality 6" GaAs substrates: Their quality is improving - - the key area of attention is related to slip formation due to stress non-uniformity in the larger-diameter wafers. We believe that this problem can be solved quite readily.

CONCLUSION

In conclusion, 6" epitaxial device wafers for microwave and telecom circuits are now possible. The production technologies and controls for such wafers are in place for 4" wafers and soon for 6" wafers. HBT scalability may be more straightforward due to the device wafer provider's ability to control device parameters across the entire wafer. FET and PHEMT circuits may benefit from the use of InGaP layers to maintain threshold voltage uniformity with good yield. It is very likely that 6" production device wafers will be widely available in the year 2000, further fueling the rapid growth of advanced circuits for wireless and broadband communication applications.

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