Effects of Ballast Resistors on Power and ESD Performance in AlGaAs/GaAs Heterojunction Bipolar Transistors

Charles Y. Chu, Jerry J. Sheu, and G.P. Li
Department of Electrical and Computer Engineering
University of California, Irvine, 92697
E-mail: cchu@newport.uci.edu, Tel: (949) 824-2047, Fax: (949) 824-3732
W. J. Ho, H. Y. Hsu, T-M Kao, C. Hua, and Ding Day
Network Device Inc., 1230 Bordeaux Dr., Sunnyvale, CA 94089-1202 © 1999 GaAs Mantech

Abstract

The effects of ballast resistors on design tradeoff between forward bias ESD robustness and peak power handling capability were studied for the first time in power AlGaAs/GaAs heterojunction bipolar transistors. It is found that though a ballast resistor prevents transistors from the current gain collapse to achieve a better thermal stability at higher power density, it can also significantly reduce the forward biased ESD performance of the ballasted junction. A design criterion for optimizing ESD survivability and output power is explored.

Introduction

AlGaAs/GaAs heterojunction bipolar transistors (HBTs) are finding increasing applications in analog, digital, and microwave circuits and have demonstrated superior power performance at microwave frequencies. While much work has been done to address the reliability issues on single emitter finger HBTs under normal operation conditions, only have a few reports focused on the electrical overstress issues—such as ESD events taking place during virtually any step of device processing, packaging, testing, and use. Unlike silicon technology where over the years tremendous amount of work has accumulated a sufficient data base on ESD protection, many of the critical ESD design parameters concerning compound semiconductor devices are still missing.

Power HBTs are typically designed in a multi-finger configuration with ballast resistors to achieve a better thermal stability at higher power density. In addition to sharing the same concerns about the reliability and ESD protection as other compound semiconductor devices do, power HBTs need to include the effects of ballast resistors into the reliability and performance consideration. In this paper we will investigate the effects of ballast resistors on power and forward bias ESD survivability of the multi-fingered AlGaAs/GaAs heterojunction bipolar transistors.

Experimental Setup

In order to get a further insight into device performance in ESD regime, an ultra low impedance transmission line pulsing technique (ULZTLP) is used (Figure 1). It mainly consists of an ultra low impedance transmission line (3.12 Ω), a high quality mechanical switch, a termination network, a high voltage power supply, and a high bandwidth oscilloscope to capture the current and voltage pulse waveforms. Using a specially constructed ultra low impedance transmission line, high frequency oscillation is suppressed by the skin effect, while DC pre-charge voltage is significantly reduced. Since the voltage requirement in ULZTLP is eased, it is particularly suitable for wafer level ESD evaluation.

The typical current pulse waveform for a 1 Ω resistor under a 2 A pulse is depicted in Figure 2 illustrating an overdamped current waveform suppressing high frequency oscillation in TLP. A sequence of monitored stress current pulses along with the corresponding voltage drop is then used to generate an IV curve, which can be correlated to ESD stress conditions and is an indication of the performance of the protection device. The ESD testing results on output NFET's and diodes in silicon using ULZTLP correlate well with traditional 50 Ω TLP and ESD HBM techniques. In general, it has a 1:2 correlation to HBM peak discharge current.

Results and Discussions

Failure mechanisms

The typical device layout of multi-fingered HBTs is shown in Figure 3, illustrating emitter ballast resistors connected to the emitters. Figure 4 depicts the typical device failures in HBT's subjected to forward bias ESD stress, illustrating the ballast resistor failing before the HBT's junctions. In comparision to the characteristics of ESD and EOS type of failure, the randomness of failure sites is also observed in forward bias conditions. When ESD/EOS types of stresses induce degradation in ballast

resistors, significant damage to the dielectric layer are observed. When ESD stress duration is shorter than 1usec, the metal layer undergoes adiabatic heating process. If the ESD stress level is high enough, local temperature will rise to a level beyond the melting point of the ballast resistor material and thus cause the ballast resistor degradation.

HBTs Under Normal Operating Condition

When operating at high power density, HBT's current gain decreases with temperature, exhibiting a drop in collector current in the transistor characteristic curves. Collector current collapse robs availability of output power and limits voltage swing in RF operating condition. To improve thermal stability, emitter ballasting scheme is usually used. To evaluate the maximum output power of the HBT's, the on-set of collapsing current and voltage are measured. (Figure 5) While the HBT's without ballast resistors show collector current collapse at relatively low voltage, those with ballast resistors are improved significantly. The DC power density induced collector current collapse and maximum oscillation frequency are measured as a function of ballast resistor values. (Figure 6,7) While the DC power density improves in HBT's along with an increase in ballast resistor value, the maximum oscillation frequency drops by 10% (Figure 7). This is due to an increase in emitter resistance.

ESD Survivability

To evaluate the HBT's ESD survivability, forward bias ESD events were created between each set of device terminals: emitter-base, base-collector, and emitter-collector. ESD survivability in the reversed bias situation is invariantly low. Ballast resistors neither enhance nor worsen HBT's reverse bias ESD performance.

With ULZTLP, a stable anode voltage can easily be captured from the two terminal diode ESD testing. Figure 8 illustrates pulsed I-V characteristics of the forward bias base-emitter junction with different kinds of ballast resistor materials. It is noticed that a substantial difference in diode characteristics is observed due to ballast resistors and that self heating in a thin film ballast resistor can affect current conduction. For the base-emitter junction, forward bias ESD survivability can be reduced by as much as 70% as a result of incorporating a 3 Ω ballast resistor. In addition, the sub-collector semiconductor ballast resistors exhibit non-linear IV characteristics due to velocity saturation and self heating. This non-linear behavior further limits the junction from bleeding off higher ESD discharge current while increasing the voltage drop across the ballast resistors. Consequently a higher ESD energy density leads to degradation of ballast resistors.

The base-collector junction is not electrically affected by the ballast resistors. Its robustness is independent of ballast resistor values. Figure 9 illustrates a pulsed IV characteristics of a forward biased collector-emitter junction with base terminal floating. For the collector-emitter junction stress, a combination of junction and ballast resistor failure is observed. Junction can become more leaky before the ballast resistor fails. The normalized forward biased ESD survivability is plotted as a function of ballast resistor values for base-emitter, base-collector, and collector-emitter junctions, respectively in Figure 10. It should be very clear by now that the higher value of ballast resistors is used to achieve higher RF output power, the worse the HBT's ESD survivability would become. Thus a proper design value of the ballast resistor should be carefully chosen to optimize the output power and minimize the ESD vulnerability.

Conclusion

While ballast resistors can improve AlGaAs/GaAs HBT's thermal stability and RF output power, it may have adverse effects on the forward bias ESD survivability. Different materials, which have a higher threshold in current density for ESD failure should be evaluated as an alternative for constructing ballast resistors. In light of the ESD survivability degradation due to a higher value of ballast resistors, the emitter ballasting scheme might be a better choice than that of base.

Reference

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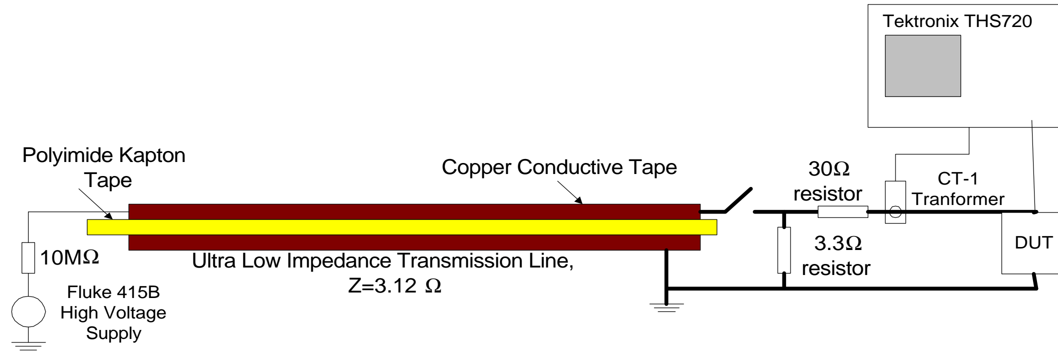


Figure 1. Ultra low impedance transmission line pulser(ULZTLP) setup.

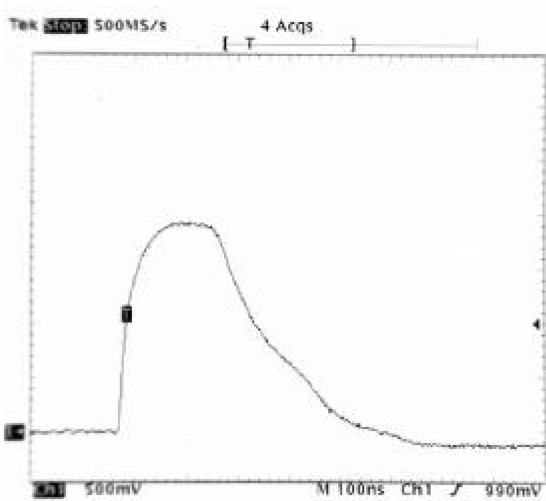


Figure 2. Ohmic voltage drop across a 1Ω resistor under a 2A current pulse. The waveform is overdamped, the rise time is 40ns.

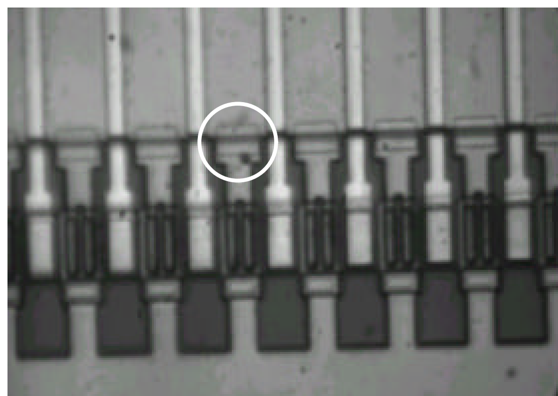
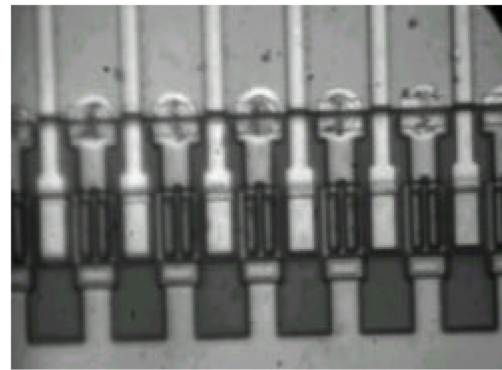


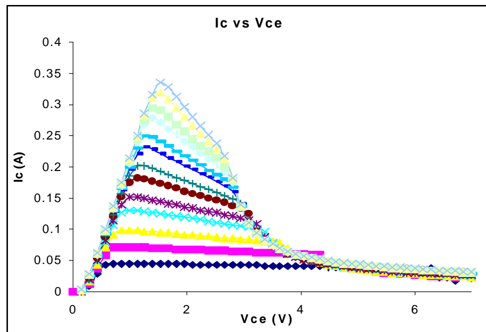
Figure 3. Typical multifinger power HBT layout with ballast resistor (in white circle).



(a)

(b)

Figure 4. (a) Typical failure in ballast resistor when forward bias zap between collector and emitter junction. (b) Typical failure in ballast resistor when forward bias zap on base and emitter junction.



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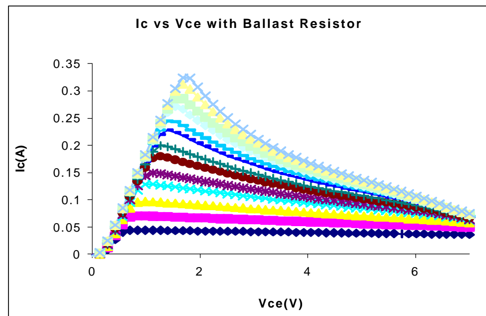


(b)

Figure 5. (a) Collector current collapse in HBT's without ballast resistor. (b) HBT with ballast resistor showing no signs of collector current collapse.

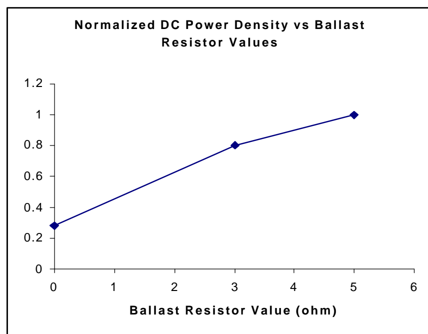


Figure 6. Normalized DC power density with respect to ballast resistor values.

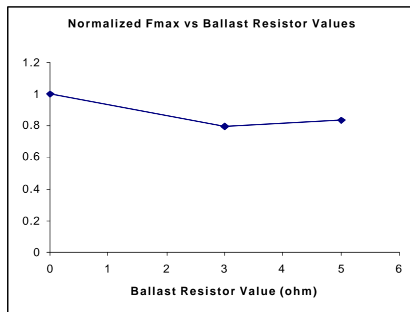
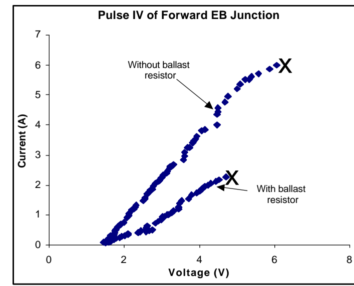
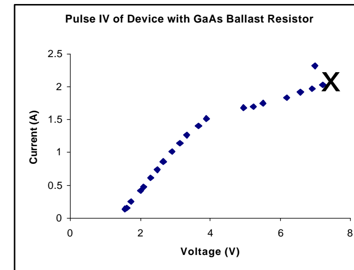


Figure 7. Normalized Fmax with respect to ballast resistor values.



(a)



(b)

Figure 8. (a)Pulse IV of forward biased EB junction. The last points marked by X's indicate failure points. Notice ballast resistor significantly reduces the robustness of EB junction forward bias zap. Blown ballast resistor leads to early failure. (b)Semiconductor ballast resistor shows velocity saturation at high current.

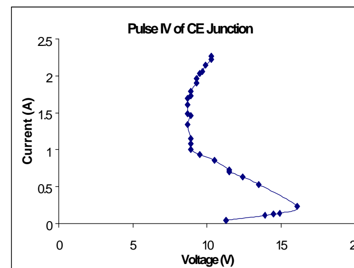


Figure 9. Pulse IV of forward biased CE junction.

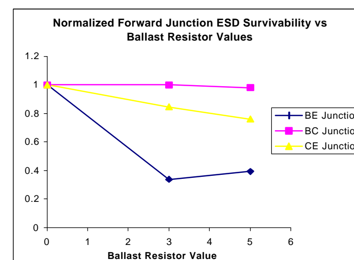


Figure 10. Normalized forward junction ESD survivability with respect to different ballast resistor values. Notice BE and CE junctions are significantly affected, while BC junction remains unchanged.