An Efficient On-Wafer Production Test System for MMW Power MMICs with Diagnostic Flag Capability

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Abstract

An on-wafer production test system has been developed which provides 100% dc and rf screening of millimeter-wave power MMICs to customer specifications. The test software is modular making it easily adaptable to unique customer requirements and is attached to a linked database for rapid data analysis and chip delivery. A principal feature of the system is its sophisticated network of failure flags which are used to highlight potential processing/design problems. The flags are linked to a series of diagnostic tests performed on every MMIC in addition to the usual rf measurements such as power output, gain and drain/gate current. The diagnostic tests screen out non-compliant MMICs before RF test thereby minimizing test time. Pareto analyses will be presented showing the utility of the flags in diagnosing specific processing problems.

Introduction

Millimeter-wave systems operating at frequencies up through W-band are flourishing. Principal military uses of these frequencies include missile seekers, fire control radars and secure communication links. Commercial products include collision avoidance systems for automobiles, line-of-sight communication links for cellular base stations, wireless LANs, local multipoint distribution systems (LMDS), personal communications network (PCN) links and satellite communications systems. Northrop Grumman has successfully fabricated PHEMT power MMICs that have been placed into several of these systems [1]. To effectively deliver the production quantities of MMICs needed, a test system was developed that; 1) allows 100% nondestructive on-wafer dc/rf screening of millimeter-wave PHEMT power MMICs, 2) is efficient and minimizes test time, 3) is easily expandable and adaptable to specific customer needs, 4) incorporates a sophisticated failure flag system that highlights potential processing/design problems and 5) attaches to a linked database system to provide expedient MMIC level data analysis and chip delivery.

Description of On-Wafer MMW Test/Failure Flag System

The new test system described here provides 100% on wafer dc/rf screening of all MMICs. The previous test software did not retain relevant dc data for failed MMICs and often lacked in flexibility to adapt, easily, to unique customer specifications or requirements. The design of the new test software is modular and can be easily expanded to fit changing customer needs. One of the primary features of this test system is the fast and efficient method used in measuring the devices.

The physical implementation of the on-wafer test system is fairly typical. It's a scalar rf power/dc measurement setup using high quality components to maintain accuracy and repeatability. The setup basically consists of a swept frequency MMW signal source followed by a solid-state amplifier to achieve the desired input power levels to the MMICs, a high directivity input coupler to sample incident power, cabling and rf wafer probes to connect to the MMICs on-wafer and an output power meter to measure MMIC power output. Meters monitor dc voltages and currents at both the gate and the drain. The drain voltage can be applied either pulsed or CW depending on the specific MMIC application(e.g., commercial vs military).

A flowchart showing the sequence of tests performed on every MMIC is given in Figure 3. In addition to measuring fundamental performance parameters such as power output, power-added efficiency(PAE), drain current and gate current vs frequency and input power level, the test software also measures breakdown voltage(BVgdo), Idss, dc gm at the bias point and gate bias voltage. The test software is of a "modular" design, meaning that subprograms are called in the program main body to perform specific measurements such as breakdown voltage for example. This allows the software to be easily expanded, as needed, to accommodate a specific test or spec requirement.

Flag Number	Failure	Failure Conditions
0	MMIC passed all on-wafer screening tests	N/A
1	Excess leakage current(initial leakage test)	Id > Ileakage_max
2	Low breakdown voltage	BVgdo < BVgdo_min
4	Drain open	Idss < Idss_min
8	Drain shorted	Idss > Idss_max
16	Gate shorted	Ig < Ig_dc_min
32	Bias failed	Failed to bias at specified % Idss
64	GMDC too low	Gmdc < Gmdc_min
128	Gate shorted - DC	Ig < Ig_dc_min
256	Gate shorted - RF	Ig < Ig_rf_min
512	RF gain too low	Gain < Gain_min
1024	Excess leakage current(final leakage test)	Id > Ileakage_max

Table 1. Failure flag codes and test conditions.

An extremely important feature of the new test software is its system of failure flags. A summary of the principal failure flags and their meanings is given in Table 1 while the flowchart in Figure 3 depicts where the flags are recorded in the overall test sequence. The failure flag system consists of a series of binary weighted codes, specific to the type of failure or failures. These flags are set if the MMICs do not meet minimum on-wafer dc and/or rf screening requirements dictated by the customer specific test plan. Multiple failures are flagged, uniquely, by simply adding the binary flag numbers. For example, if a MMIC fails the Idss measurement due to both a gate and a drain short, it is flagged with failure code 24, 8 for the drain short plus 16 for the gate short. Once a MMIC is flagged for failure, the data accumulated to date is recorded, further testing of the MMIC is stopped and the test software jumps to the next die site. Noncompliant MMICs are therefore weeded out as soon as possible thereby minimizing test time. All measured parameters(dc,rf and failure code) are sent to a database so that queries can generate customer "picklists" of spec compliant die or yield/Pareto analyses can be performed[2].

Diagnostic Test/Flag Analysis

A number of the standard diagnostic tests performed on the MMICs as part of the production testing has proved invaluable in making MMIC delivery more efficient and less costly. In addition, the diagnostic flags have been used to monitor, identify and correct production line design/processing problems.

One diagnostic test incorporated into the test software to prescreen the MMICs is called the "leakage test". This test, performed first and last in the measurement sequence(see Figure 3), measures the amount of drain "leakage" current

of a pinched-off MMIC. The test is performed after the MMIC has passed the rf testing to ensure that there was no latent damage done to the chip after the rf was applied. Regardless if the MMIC passes the test or not, the leakage current is measured and recorded. The principal use of the leakage measurement is to reduce the number of defective MMICs sent to QC visual inspection. In the past, a MMIC which passed all on-wafer screening and rf specifications could fail at QC visual. One of the main causes of QC rejection was for missing gates, especially on the large power amplifiers. A 1.5W Ka-band power amplifier currently being produced, for example, has 144 0.25um T- gates. The magnification level required to inspect a gate is greater than 500X and the time to visually inspect for missing gates is about 1 minute per MMIC. This type of inspection is, obviously, tedious and very labor intensive. The leakage measurement has helped significantly in alleviating the throughput and cost impact at QC. Now, queries can be designed to preselect devices that have less than a desirable amount of leakage current before going to visual inspection.

Another benefit of the failure flag test system is that it provides discernible data that can clearly separate out the better performing MMICs. The entire failure flag system is incorporated into the test measurements and is sent to a larger database. From the database, Pareto analysis is performed to determine dc/rf yield losses. This data gives engineers insight into wafer specific processing problems. For example, certain flags indicate poor gate adhesion,

others suggest a misregistered channel/gate alignment or poor breakdown performance. Interpretation of the flags is important and can serve as a visible tool in addressing and resolving yield issues. Figure 1 is an example of a Pareto chart used to show a separation of all dc failures for a typical wafer. Pie charts, as shown in Figure 2, give engineers insight into wafer specific problems. For example, Figure 2a depicts a wafer with 40% of the devices failing for excessive leakage current. This failure flag, as described previously, corresponds to a significant number of 0.25um T-gates missing per MMIC. Figure 2b is a Pie chart depicting low breakdown voltage performance on a wafer. A large percentage of the MMICs failed to either bias up at a certain drain voltage or were destroyed after the final rf measurement. Another analysis tool that has helped engineers address yield issues includes the ability to wafer map key failure flags. This procedure helps to highlight uniformity and/or processing trends across the wafers. These charts and maps of failure flag codes were essential in identifying key production problems and contributing to overall processing yield improvements.

Summary

A novel on wafer test system has been discussed. The system includes modular test software which provides the flexibility to adapt, easily, to customer specifications or requirements and has rendered increased visibility for MMIC design, processing, and test. In addition, the test routine contains a very sophisticated failure flag system that is used to identify key processing yield issues. The system has been very instrumental in achieving recent dc/rf yields as high as 50% for a 1.5W Ka-band power amplifier currently in production.

References

1. R.G. Freitag, K.M. Renaldo, H.G. Henry and J.E. Degenford, “MMIC Amplifier Chip Sets for Ka-Band Military and Commercial Applications,” 1997 GOMAC Conference Digest, pp. 185-188.
2. K.M. Renaldo, J.W. Atkinson, S.F. Rutz, S.P. Spurgeon and H.G. Henry, “Electronic Database for MMIC Design Traceability,” 1998 Proceedings on GaAs Manufacturing Technology(MANTECH), pp. 115-117.

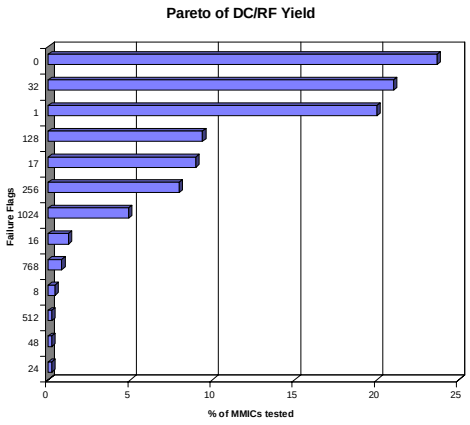

Figure 1. Pareto analysis of dc/rf failure flags for a MMIC wafer.

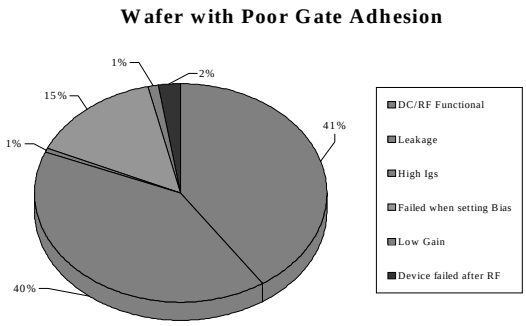

Figure 2a. Pie chart depicting a wafer with poor gate adhesion.

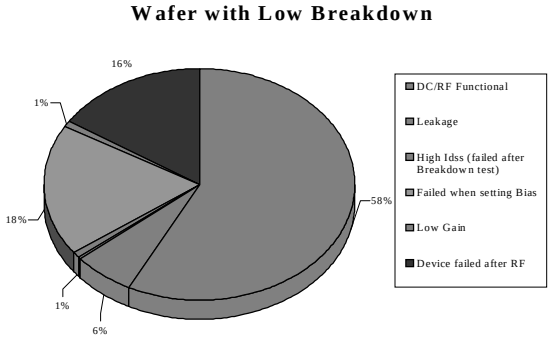

Figure 2b. Pie chart depicting a wafer with low breakdown.

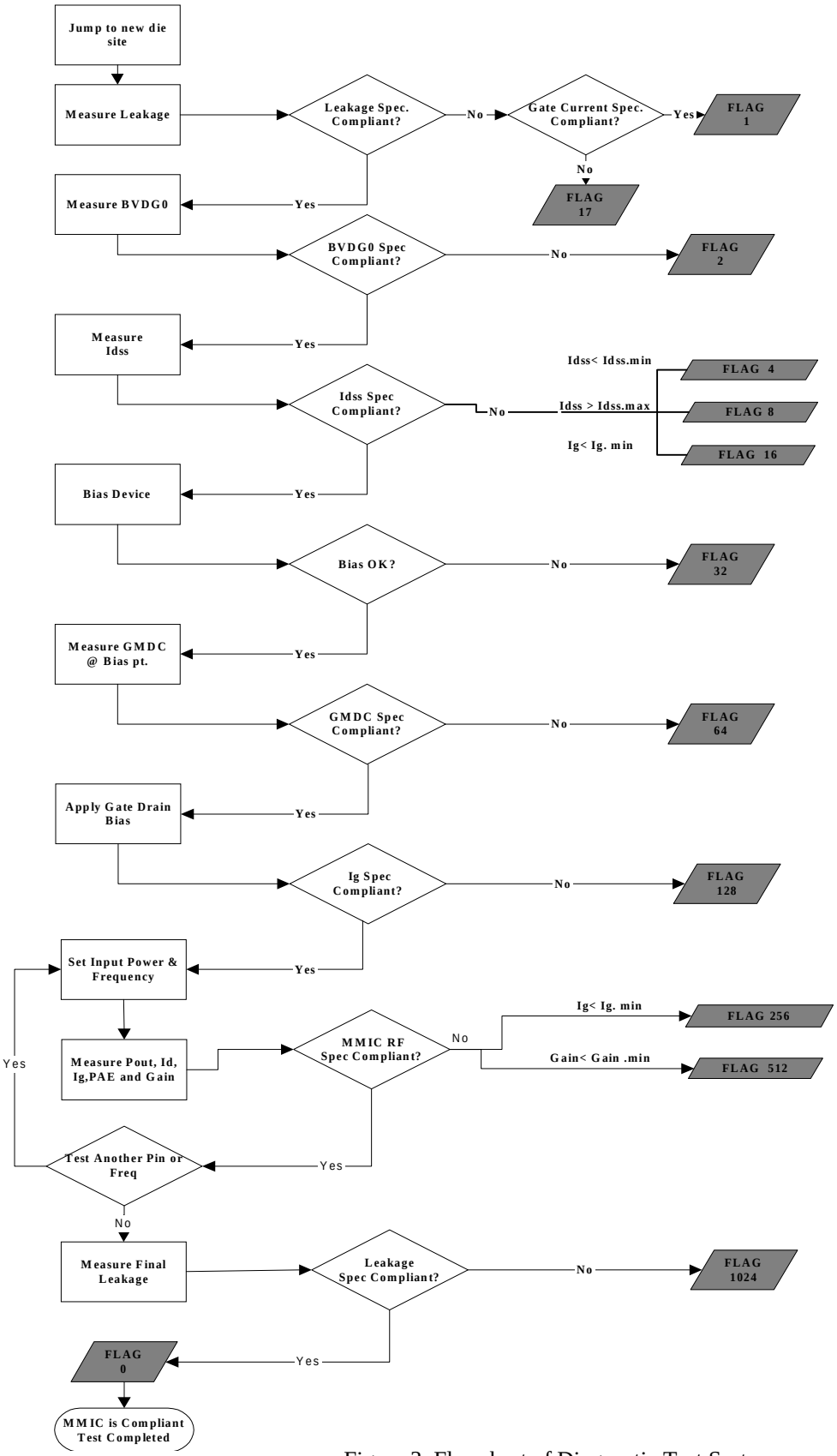

Figure 3. Flowchart of Diagnostic Test System.