Packaging of Ultra-Thin Film GaAs Devices for Increased Thermal Efficiency and High Density MCM's

Mike Sickmiller, Alex Pike, Steve Jacobs, Luan Vo, P.
Pete Zampardi*, Gerry Sullivan*, Brian McDermott*

ELO Technologies, Inc.
3205 Ocean Park Blvd. Ste 180
Santa Monica, CA 90405
Phone: (310) 452-6688 Fax: (310) 452-9188
sickmill@ELOtechnologies.com

*Rockwell Science Center
Thousand Oaks, CA
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ABSTRACT

A major concern in GaAs and high density MCM packaging is thermal density. Thinning of the GaAs substrate alleviates this problem somewhat, but current thinning techniques are limited to about 100 µm. The thickness of the substrate adversely affects heat sinking as well as requiring long through-substrate vias for electrical interconnection to the backside of the chip.

Using the ELO Packaging Process, the substrate can be thinned to only a few microns. This eliminates the long thermal path, makes vertical interconnects short and easy, and in many cases increases the electrical performance of the device itself through the elimination of substrate parasitics.

INTRODUCTION

Epitaxial Liftoff (ELO) Packaging is the processing and packaging of extremely thin crystalline semiconductor films. This is done by removing the semiconductor substrate after fabrication of the devices on the wafer [1]. This new manufacturing process opens the door to a multitude of applications including higher power chips, higher frequency devices, chip stacking, and high efficiency opto-electronic devices [2].

Presented here is an Epitaxial Liftoff Packaging Process flow for packaging of high power devices and high density MCM's through solder bonding of the thin film devices and chips to virtually any substrate. The process uses standard flip chip equipment and technology, but process modifications have been introduced to accommodate the extremely thin device structures. The techniques to bond the circuits to heat sinks, transparent substrates, or flexible substrates are presented.

An ultra thin film processing and handling technique enables the packaging of active semiconductor devices as thin as a fraction of a micron. Using this ELO Packaging Process, a wide variety of devices and electronics can be fabricated for advanced high circuit and power density applications.

PROCESS FLOW

By removing the substrate of a semiconductor chip, we eliminate the long thermal path which impedes heat sinking of the active circuitry. The resulting increase in heat sinking efficiency provides lower device operating temperatures on chip, which lead to high efficiency, higher linearity, higher circuit densities, potentially longer life and higher reliability, and lower cost cooling systems.

The ELO Packaging Process is completely compatible with existing GaAs foundry processes. The process is inserted between the GaAs Fab and packaging house, requiring no customization at either end for most chipsets. Utilization of the ELO Packaging Process may open doors to device redesign, wafer layout, and other engineering implemented on the front end which can increase both device performance and wafer yield, however,

such designs are not prerequisites to integrating the Process [3].

Once the GaAs wafers are fully processed in a conventional foundry, further chemical processing is implemented to begin the ELO Packaging Process. A single, low resolution photolithography step is required which defines the actual chips. The subsequent etch step essentially replace the dicing or scribing step which would occur in a conventional packaging process. The etch, however, is only performed to a distance of several microns, allowing us to handle the semiconductor while it remains in wafer form.

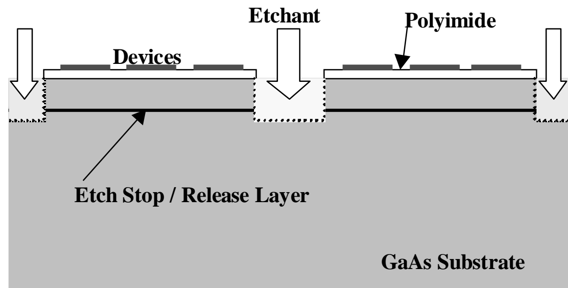

Figure 1. Etch to define dice on wafer

The next step is the attachment of an intermediate carrier substrate (or "superstrate") to the topside of the fully processed wafer. A liquid polymer is dispensed onto the surface of the wafer, the wafer attached to the intermediate carrier and the polymer cured. This method gives us a robust process which will withstand somewhat harsh processing steps.

Now that the GaAs wafers are attached to the carrier, this carrier may be treated like the wafer itself. The system is then flipped over and the backside of the GaAs wafer is processed. A substrate removal etch is performed, thinning the wafer to only a few microns of thickness and in the process separating the individual die from each other. Inherent AlGaAs layers within the GaAs die act as an etch stop providing etch selectivities to 1000:1 and higher, resulting in precise thickness control of the die [4]. All the while, these ultra-thin die are supported by the intermediate carrier substrate.

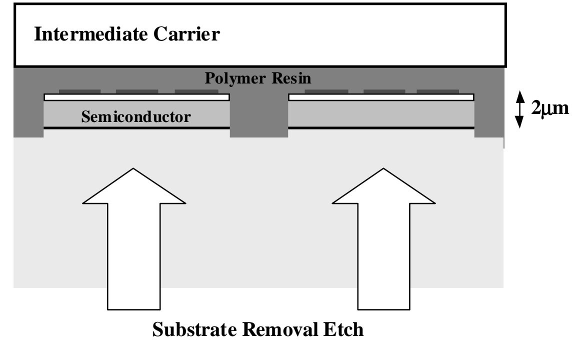

Figure 2. While the wafer is supported by the Intermediate carrier, the substrate is chemically removed resulting in the formation of the individual dice.

With the substrate removed, we can perform advanced processing steps on the backside of the die as a batch process – because the die are still arranged in the wafer layout. Photolithography, etch, and low temperature material deposition are all feasible at this stage. Etch pits may be drilled from the backside for thermal or electrical vias to contact bus line on the front of the dice. Solder pads have been evaporated for subsequent attachment to thermally sinking packages. Such pads may be deposited on the entire backside of the die or selectively patterned using photo-lithography.

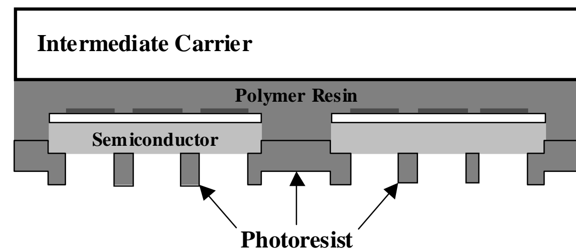

Figure 3. Photolithography and other processing steps can then be performed on the backside of the devices.

Using high resolution flip chip packaging equipment, these ultra-thin chips have been bonded to AlN heat sinks with only a few microns of solder.

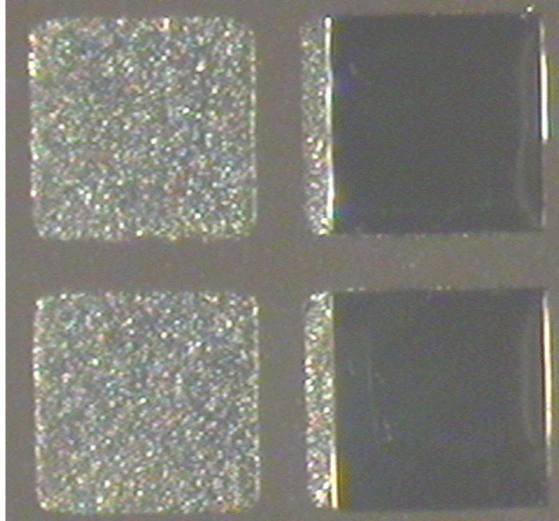

Figure 4. Bonded ELO ultra-thin films on the right next to open solder pads on the left.

The resulting extremely short, and highly thermally conductive path essentially reduces the heat path from the device junction to the heat sink by an order of magnitude. The resulting lower junction temperatures provides increased linearity, gain, and efficiency for high frequency devices. Similarly, this advanced heat sinking will aid in high circuit density packages such as stacked Multi-Chip Modules.

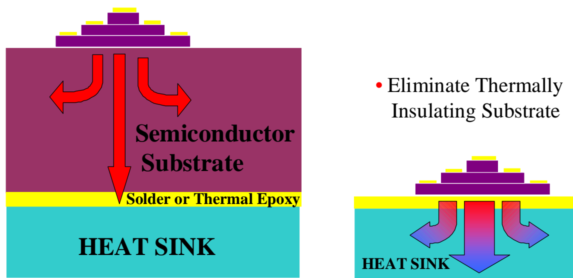

Figure 5. The reduced thermal path from device junction to heat sink increases the heat sinking capability of the package.

The process compatibility has been proven with commercial production Power Amplifier chips (PA's) obtained from Rockwell Semiconductor. Production wafers of 1.9GHz PA's were processed and thinned to 2 µm. Solder pads were deposited onto the backside of the dice and they were bonded to an AlN heat sink with only 2 µm of solder.

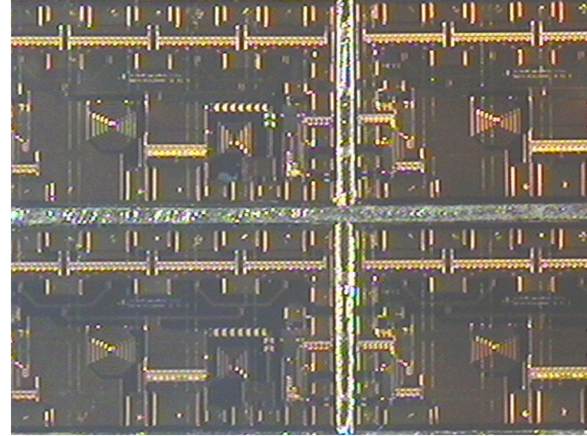

Figure 6. Bonded ELO ultra-thin (2 µm) Power Amplifier chips from Rockwell Semiconductor

SUMMARY

We have developed a manufacturing process flow for the fabrication and packaging of extremely thin GaAs devices and chips. By implementing this process for high power chips, we can shorten the thermal path between the device junction and heat sink by an order of magnitude. The resulting lower operating temperatures of the device will increase gain, linearity, and efficiency of the devices, reduce package size and potentially cost, increase the reliability and lifetime of the device, and increase the available power density of the package.

As a result of the techniques developed here, GaAs devices can be processed on the backside creating new device designs, 3D chips or MMICs, and vertical interconnections between stacked chips. Such backside processing technology coupled with the thermal advantages described here will enable ultra-high density stacked chip MCMs.

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