

# The Siemens 150mm GaAs Production Facility

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## SIEMENS GOES FOR SIX

For the first time the GaAs device suppliers are confronted with a real global market and an extraordinary dynamic business, that of wireless communication. The specific features of this market are permanent system innovations, steep production ramp-up curves and price levels of a consumer market.

A copy of the successful Si approach, i.e. 100% production orientation and flexibility combined with innovation leadership, can only manage this challenge.

Today Siemens and handful suppliers in USA and Japan realise a production volume of 40K 4"-wafer starts per year. This corresponds to a production volume of more than 70 Mil components in 1998, of which more than 50% are MMICs.

To meet the requirements of tomorrow, i.e. to exceed the market CAGR of 30% predicted, and to develop its leading position in the area of RF products, Siemens will open a new 6"-GaAs fab in 1999 (building H95 in fig.1).

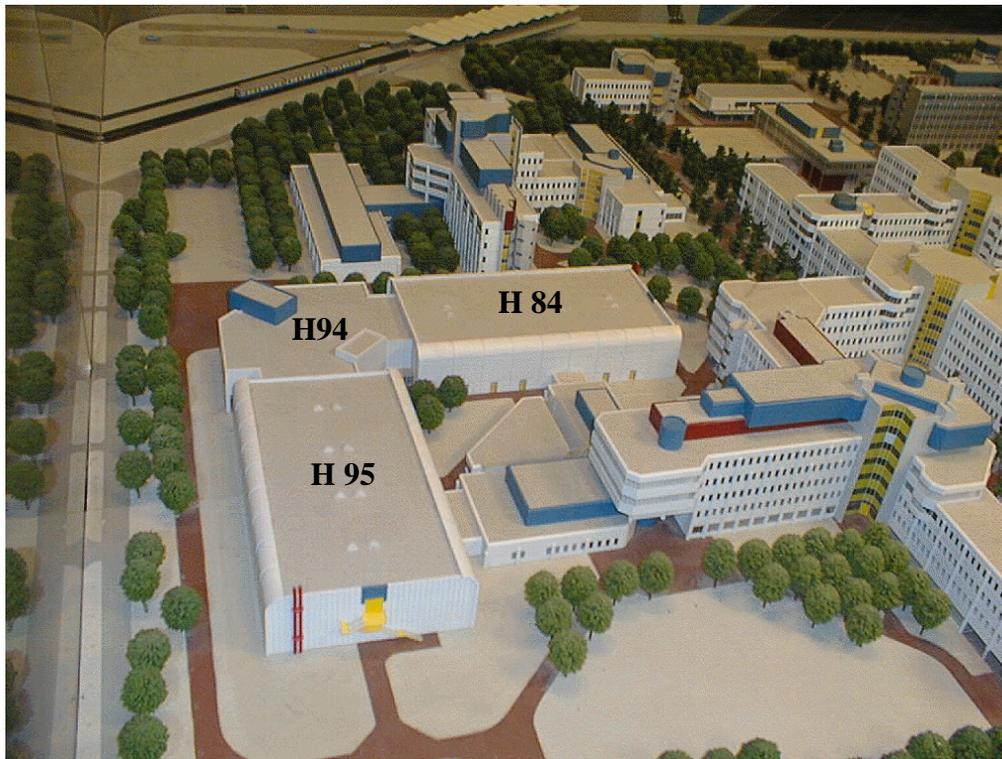


Figure 1: RF Wafer Fab, H95 GaAs frontside, H94 GaAs backside, H84 Si-Bipolar

This will be the first 6"-GaAs fab for analogue chips. The wafer fab is located in Munich Perlach, where Siemens concentrates its RF 6-inch wafer facilities, i.e. production synergies to the Si & SiGe Bipolar/MOS/BICMOS lines (H84 in fig. 1) and the new Sensor micro-machining lines are part of the business strategy.

The challenging time schedule started with the preparation of the already existing class 10 clean room in the second half of 1998. Ready for equipment was already passed in Nov. '98 and ready for process was reached in Jan '99. Thereafter R & D has started. Start of production is foreseen for October 1999. As soon as possible all three GaAs process technologies, MESFET, HEMT and HBT, will be transferred completely to 6-inch.

#### FACILITY

The GaAs facility building was erected already a few years ago dedicated at that time to the development and production of 1MB / 4MB DRAMs. In H95 about 2100m<sup>2</sup> class 10 clean room space is available. This total area is split between the GaAs (1200m<sup>2</sup>) production and the expansion of the Si (600m<sup>2</sup>) operations from H84. Either the GaAs or the Si production can expand into the remaining free space. The backside and it's

associated processes are performed in about 150m<sup>2</sup> of H94. The wafer test area is not included here because this is integrated within the GaAs/Si testing area located on the same fab site.

The layout of the building is state of the art with a 3-floor concept. In principle is a two building recipe. The inner building being the class 10 clean room itself. The lower floor (basement) carries all infrastructure installations. Gas and DI wafer supply, the drains, vacuum pump stations and main equipment aggregates that are not necessarily to be placed in the clean room adjacent to the tools. The clean room floor itself is low vibrational due to it's separate grounding except to the outer 2m from the clean room walls. The third floor carries all the air ventilation technique.

The clean room is divided into 18 sections. These sections have nearly independent air ventilation from the third to the first floor. The air is pumped from the third floor through the filter ceiling into the individual sections. It passes as laminar flow through the clean room and the perforated floor and is recirculated via the air channel between the outer and the inner building back to the third floor. (fig.2)

The laminar flow pressure in the clean room can be adjusted for each 60cm x 60cm field. This allows to reduce the flow in the service area behind the tools for cost saving.

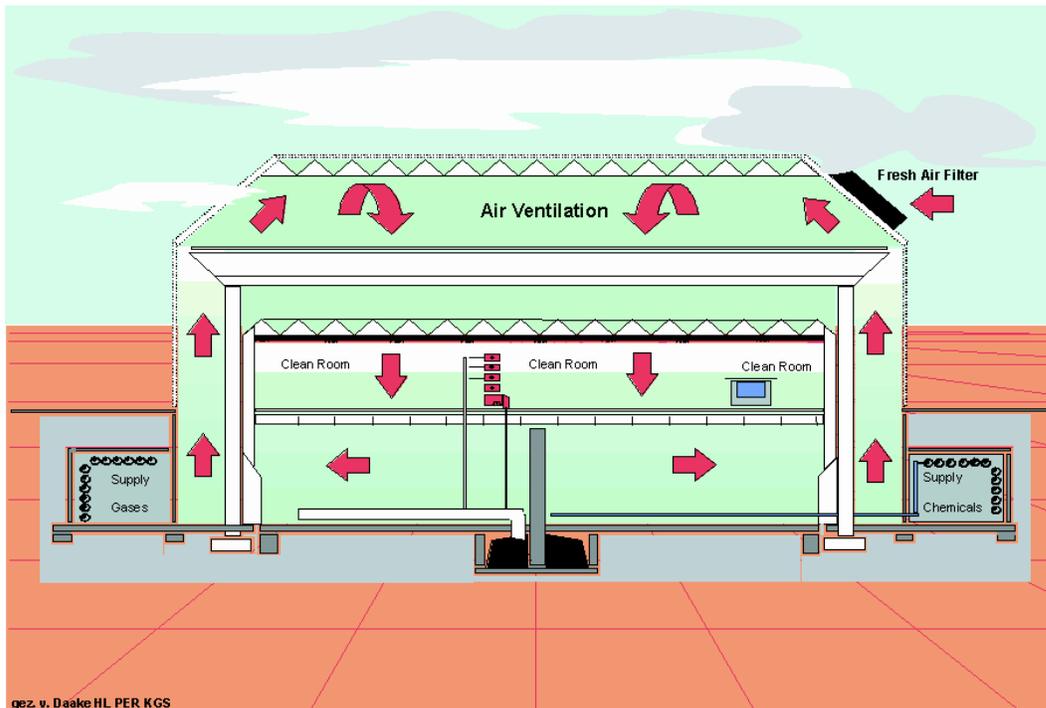


Figure 2: H95 GaAs Facility schematic

The building has two separated media supply basements (see figure 2), one for gases and one for chemicals. The media in general are fed from central supplies. The GaAs and the Si facility are supplied from a joined central supply and for those media, only used for the GaAs processes, separate supplies were installed.

The air ventilation, all gas and chemical supplies can be shut down independently in each section in any case of emergency. The safety precautions required for the GaAs production facility have been rechecked for the special requirements. In some cases additional activities are necessary, specially has to be taken to avoid any GaAs contamination spreading.

Special care has been spent to avoid any possible contamination of GaAs into the Si productions. The presence of any GaAs wafer in the Si production area is strictly forbidden. For Si- wafer a one way only concept is implemented that guaranties that Si-wafer processed in the Si facility can be transported into the GaAs facility but the way back is completely blocked.

#### EQUIPMENT

The planned tool set in the line is oriented to a capacity of 1000WSPW (Wafer Starts Per Week) 6" in phase I. The capacity can be upgraded in phase II to process up to 2000WSPW in the planned clean room area. After this expansion there is still free space left to enlarge either the GaAs or the Si processing capacity.

The front side and backside processes including thinning and via hole technique are covered in H94 and H95. The wafer sawing before assembly will be done at the assembly backend locations.

For Si-Bipolar and the sensor micromaschining a few process steps will be integrated into the GaAs operations. Mainly the special Au based metallisations and etching procedures are not available in the Si line.

The production equipment used in the existing 4" line is already dedicated to volume production and the equipment selection is oriented to the Si main stream equipment road map. For the 6" tool set this strategy was further expanded. Equipment teams were engaged with members of the GaAs process and production, 6"-Si process and production and maintenance personnel from GaAs and Si, respectively. These teams bring together the most possible synergies between GaAs and 6"-Si volume production experience. The corporate purchasing was also represented.

The premises for the tool selection were:

- proven process according spec on 6" GaAs wafer
- the lowest Cost of Ownership
- highest synergies to the existing 6" Si fab for maintenance and equipment suppliers
- refurbished tools
- compliance to delivery schedule

With a set of documents potential equipment vendors were invited to participate in the tool selection process: the Basic Purchase Agreement, Non Disclosure Agreement, Request for Quotation, Development Agreement and the Siemens Cost of Ownership Document. In principle there was a high interest in most of the Si main stream equipment manufacturer to serve also the GaAs industry.

The basic problem for a few manufacturers was the stringent requirement of running GaAs wafer for process evaluation and verification of problem free mechanical handling of GaAs wafer in the tool. They were very restricted because of the GaAs contamination in their Si oriented application labs. Therefore the very first tests were performed on Si wafer to demonstrate the process capability of the tool. But finally we got the process spec verified on GaAs wafer.

The main problems faced during the selection process:

- robot handling of GaAs wafers in cluster tool
- temperature stress  
(Si process mostly at higher temperatures with higher deposition/etching rates)
- temperature management in the handling had to be refined

Finally all the information gathered for each tool in the evaluation procedure was put into a formal decision matrix. This matrix gave condensed data not only for the fulfillment of the requirements but also for possible risks and uncertainties. The equipment board finally decided.

#### SUBSTRATE MATERIAL

In the first evaluation tests 6" wafers with notch and flat were processed e.g. on a resist spinner. We decided to use notched wafers. This is required because of the unacceptable vibrations transferred to spinning axes at higher spinning speed because of unbalance caused by the non uniform mass distribution of the heavy weight 6" GaAs wafer with flat. For Si this was decided for 8" wafer. The notch orientation is located at the [010] direction. Discussions were lengthy for the decision on DSP (Double side polished) or SSP (Single Side polished) surfaces. The Si 200mm spec is DSP.

The electrical spec for 6" will be identical to our qualified 4" spec.

Material from a couple of vendors has already been tested in the early program phase. The basic 6" material quality was analysed by processing 4" wafer cut off centre out of 6" wafers. The homogeneity in ion implantation process to our standard contact and several channel implant schemes were tested. 6" material shows excellent homogeneity (fig. 3).

Further 4" out of 6" have been fully processed including extensive DC and RF analysis. The results are also excellent, taking into account that these results could be achieved without any process refinements. It is clear that these data are not a release of the material, because all diameter dependent process influences are not yet known and reliability analysis is not completed. But it gives a very good basis for the process transfer to 6".

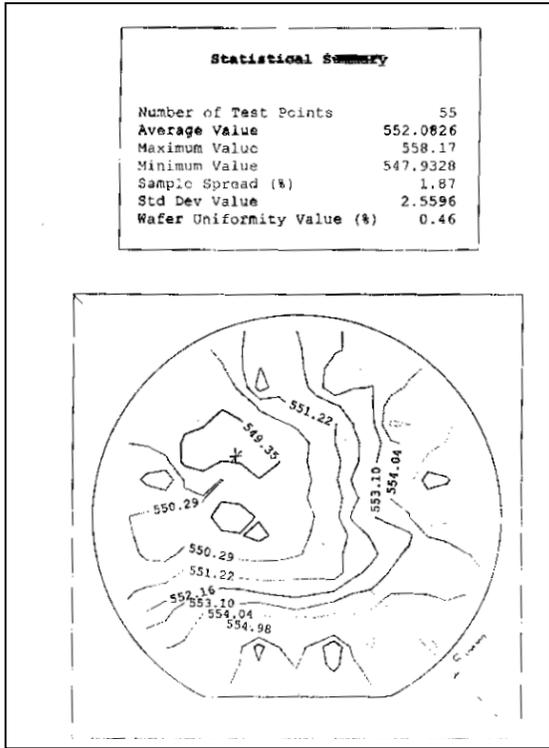


Figure 3: 4" out 6" sheet resistance contour plot

#### ACTUAL STATUS

In the actual status (Feb. '99) of the process transfer to 6" most of the equipment is installed. The equipment installation and process set up was very smooth. Thanks to the extensive qualification procedure and tight equipment supplier involvement in the procurement phase. The single processes are in the verification phase and are before internal qualification. Only a single tool is missing, scheduled for Aug. '99. However, using a loop with the 4" fab that is also located in Munich the MESFET process can be run completely. The first mask sets for qualifications of the complete process and for customer sampling are in the fab. The milestone first GaAs out is expected for 15th May 1999.

Further results on the electrical data of the active FET will be given on the conference.

#### ACKNOWLEDGEMENT

Many thanks to Mr. D. Baur for managing the GaAs process group and his intensive engagement in the layout of the clean room. Mr. G. Woerndl and his team for his co-operation and the installation of all infrastructure and tool hook-ups. Last but not least we appreciate the enthusiasm and effort of all the teams infrastructure, support, purchasing, commercial, maintenance, GaAs / Si process and production.

They will make the project successful within the tight time schedule.