Gate Metallization Study for InGaP/InGaAs/GaAs pHEMTs

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Abstract

The results of a gate metallization study for InGaP/InGaAs/GaAs pHEMTs are reported. Schottky contacts with Mo/Au, Ti/Au, and Pt/Au metallizations on InGaP lattice matched to GaAs are fabricated and barrier heights of 0.603, 0.621, and 0.738 eV are obtained for Mo/Au, Ti/Au, and Pt/Au contacts, respectively. The electrical properties of 0.7 μm gate length pHEMTs fabricated with each of these metallizations as the gate contact is also reported. Threshold voltage, transconductance, f_t, and f_{max} are all found be influenced more strongly by the choice of gate metallization than can be explained by the difference in Schottky barrier height alone. A simple model that accurately accounts for the performance differences between the fabricated pHEMTs based on reduced effective gate-to-channel spacing is presented. Devices with Ti/Au gates exhibited an effective gate-to-channel spacing that was 17.5 Å smaller than identically-processed Mo/Au gate devices, while Pt/Au gate devices exhibited effective gate-to-channel spacings 47.8 Å smaller than those of Mo/Au devices.

Introduction

Pseudomorphic high electron mobility transistors (pHEMTs) are attractive candidates for use in present and emerging micro- and millimeter-wave systems because of their demonstrated high speed, low noise, and good power-handling capability. Over the last several years, there has been increased interest in the use of InGaP lattice-matched to GaAs for barrier and spacer layers in pHEMT structures, instead of the more traditional AlGaAs layers. This interest is spurred by InGaP's natural advantages for low-noise and high-power devices due to its larger bandgap (1.92 eV), absence of deep levels such as DX centers which degrade breakdown properties and increase 1/f noise, and its relative non-reactivity with air due to its Al-free composition. Although InGaP-based pHEMTs have been demonstrated with very good electrical performance [see for example 1-3], little published work on gate metallization effects for InGaP-based pHEMTs exists. In this work, an examination of the performance of pHEMTs using Mo/Au, Ti/Au, and Pt/Au metallizations on InGaP/InGaAs/GaAs pHEMT heterostructures is undertaken. The Schottky barrier properties of each of these metallizations on InGaP-based pHEMT structures is evaluated, and the properties of 0.7 μm gate length pHEMTs fabricated with each gate metal are examined and compared to the Schottky diode results.

Device Structure and Fabrication

A cross-sectional diagram of the InGaP-based pHEMT heterostructure used in this work is shown in Figure 1. The structure was grown by metalorganic chemical vapor deposition on 3" semi-insulating GaAs wafers. A room-temperature mobility of 3510 cm^2/Vs with a sheet carrier concentration of 2.1 10^{12} cm^{-2} were measured for this structure after removal of the n^+ GaAs cap by selective wet etching. Fabrication of lateral Schottky diodes and submicron gate-length pHEMTs was performed on the heterostructure shown in Figure 1 using a mix-and-match process that includes both optical and electron-beam lithography. Device isolation was performed using multiple-step selective wet etching. The n^+ GaAs cap and undoped $In_{0.2}Ga_{0.8}As$ channel were etched using a 10:1 solution by volume of citric acid and hydrogen peroxide, while the InGaP barrier, donor, and spacer layers were etched using undiluted hydrochloric acid. Due to the presence of the GaAs cap layer, the extent of lateral etching of InGaP in HCl is limited to the mesa edge, despite the very rapid vertical etch rate [4]. The exposed InGaAs channel sidewall recess was accomplished using the selectivity of the citric acid-based etch.

AuGe/Ni/Au ohmic contacts were defined by optical lithography and liftoff, and were annealed in an Ar ambient at 500 C. Contact resistances ranging from 0.08 Ω-mm to 0.1 Ω-mm were

400 Å n^+ GaAs
100 Å undoped $In_{0.5}Ga_{0.5}P$
150 Å n^+ $In_{0.5}Ga_{0.5}P$
50 Å undoped $In_{0.5}Ga_{0.5}P$
100 Å undoped $In_{0.2}Ga_{0.8}As$
5000 Å undoped GaAs
Semi-insulating GaAs substrate

Figure 1. Cross-sectional diagram of lattice-matched InGaP/InGaAs/GaAs pHEMT heterostructure.

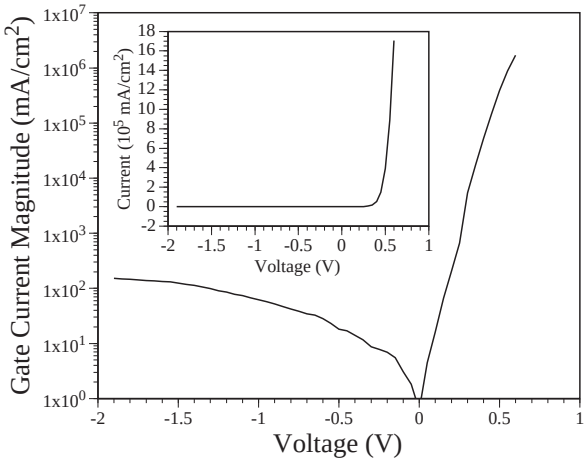

Figure 2. Current-voltage characteristic of Ti/Au-InGaP Schottky diode.

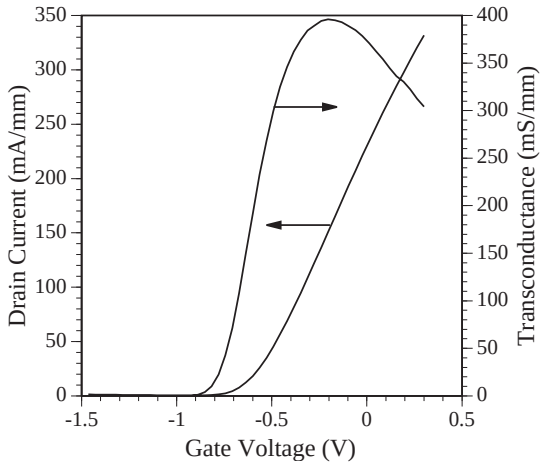

Figure 3. Drain current and transconductance as a function of gate bias for typical 0.7 μm gate length Ti/Au gate pHEMT. Peak transconductance of 396 mS/mm is achieved.

obtained from transmission-line model test structures. Schottky contacts on the lateral diodes were defined by optical contact lithography; pHEMT gates of length 0.7 μm were defined by electron-beam lithography in a three-layer PMMA/P(MMA-MAA)/PMMA resist structure. The gate recess etch process for the pHEMTs was implemented using a highly-selective citric-acid/hydrogen peroxide solution. The degree of lateral etching in the gate recess process was minimized to minimize source resistance; although this maximizes device transconductance, it is not optimal for breakdown voltage. For both Schottky diodes and pHEMTs, the Schottky contacts examined included Ti/Au, Mo/Au, and Pt/Au metallizations. In each case, the contact metal layer thickness is 20 nm, and the thickness of the Au overlayer is 200 nm.

Results

Electrical characterization of the lateral Schottky diodes was performed. Figure 2 shows the obtained log-scale current-voltage characteristic for a typical Ti/Au diode. Linear-scale current-voltage characteristics are shown in the inset. Reverse leakage current density of the diodes was found to be reasonably low, with typical values of 40 mA/cm^2 for Ti/Au contacts, 90 mA/cm^2 for Mo/Au, and 14 mA/cm^2 for Pt/Au contact metallizations. Schottky barrier heights were determined from forward-bias current-voltage measurement of diodes fabricated with the three candidate contact metallizations; the results are tabulated in Table 1. Obtained barrier heights range from 0.603 eV for Mo/Au to 0.738 eV for Pt/Au. The measured barrier heights reported here are somewhat larger than those reported previously [5], presumably due to the thicker contact metal layer in this work (20 nm in this work, vs. 10 nm or less in [5]).

TABLE 1
MEASURED SCHOTTKY BARRIER HEIGHT VS. METALLIZATION FOR METAL/INGAP CONTACTS

Contact Metallization	Schottky Barrier Height (eV)
Mo/Au	0.603
Ti/Au	0.621
Pt/Au	0.738

Direct-current characterization of 0.7 μm gate length pHEMTs fabricated on the InGaP-based heterostructure was performed with devices using Ti/Au, Mo/Au, and Pt/Au gate metallizations. Figure 3 shows typical drain current and transconductance vs. gate bias voltage for a pHEMT with Ti/Au gate metallization. A peak transconductance of 396 mS/mm and a threshold voltage of -0.586 V were obtained for Ti/Au gate pHEMTs. Identically-processed devices except for gate metallization resulted in peak transconductances and threshold voltages of 333 mS/mm and -0.694 V for Mo/Au and 420 mS/mm and -0.313 V for Pt/Au metallizations, respectively.

A typical common-source current-voltage characteristic for a Ti/Au gate pHEMT is shown in Figure 4. Similar results were obtained for pHEMTs fabricated using the other gate metallizations. In addition, on-wafer s-parameter measurements from 1 to 35 GHz as a function of drain and gate bias voltage were also measured for pHEMTs fabricated with each gate metallization. Typical values for dc transconductance, rf out-

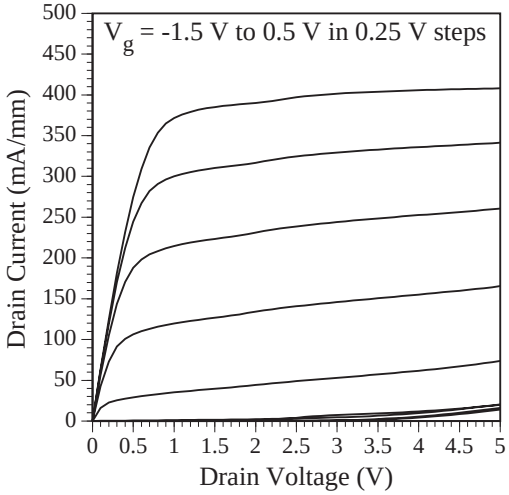

Figure 4. Common-source current-voltage characteristics for a typical Ti/Au gate pHEMT.

put conductance (obtained from s-parameter measurements with the gate biased for maximum transconductance), and threshold voltage are tabulated in Table 2. Output conductances were obtained from the s-parameter data to avoid the under-estimation of output conductance that can occur in dc measurements. Figures 5a-c show typical current gain and maximum available gain vs. frequency as obtained from s-parameter measurements for pHEMTs with Mo/Au, Ti/Au, and Pt/Au gate metallizations respectively. The f_t and f_{max} obtained from these measurements were 41.3 and 101.1 GHz for devices with Mo/Au gates, 38.8 and 93.8 GHz for Ti/Au gates, and 36.0 and 73.0 GHz for Pt/Au gates, respectively. A summary of the microwave performance obtained as a function of gate metallization is also provided in Table 2.

Verification of the high-speed potential of devices on this heterostructure was also performed. Devices with 0.25 μm gate lengths and Mo/Au gates were fabricated on this heterostructure. Excellent high speed operation was achieved, with measured values for f_t of 77.7 GHz and for f_{max} of 102.4 GHz obtained from on-wafer s-parameter measurement.

Discussion

Comparison of the Schottky barrier height data in Table 1 and the threshold voltages obtained for pHEMTs with the three investigated gate metallizations as shown in Table 2 reveals some interesting behavior. As all three types of pHEMTs were fabricated on the same heterostructure, simple theory indicates that the difference in threshold voltages between the pHEMTs of different gate metallization should be simply the difference in gate barrier heights. Tables 1 and 2, however, show a rather different picture. From the Schottky diode measurements shown in Table 1, Ti/Au has a barrier height that is 18 mV larger than Mo/Au, and Pt/Au is 135 mV larger than Mo/Au. On the other hand, the threshold voltage of typical 0.7 μm gate length pHEMTs is -0.694 V for Mo/Au gates, -0.586 for Ti/Au gates, and -0.313 for Pt/Au gates, resulting in considerably larger-than-expected threshold shifts of 108 mV from Mo/Au to Ti/Au and 381 mV from Mo/Au to Pt/Au. For conventional pulse-doped pHEMTs, the difference in threshold voltage for devices fabricated using different gate metallizations in the same material system can be found by obtaining an approximate solution to Poisson's equation in one dimension; by assuming a thin, highly-doped doping layer, the difference in threshold voltage between two pHEMTs fabricated on a common heterostructure may be expressed as

$$\Delta V_T = \Delta\phi_b - \frac{qN_d t_d}{\varepsilon}\Delta d \qquad (1)$$

where $\Delta\phi_b$ is the difference in Schottky barrier heights of the gate metals on the pHEMT barrier layer for the pHEMTs being compared, N_d is the doping concentration in the donor layer, t_d is the thickness of the donor layer, ε is the permittivity of the barrier layer, and Δd is the difference in gate-to-channel spacings for the pHEMTs being compared. The conduction band discontinuity, ΔE_c, between spacer and channel layers does not appear in the equation for threshold voltage differences since it is assumed to be common to all of the HEMT structures being compared.

For the present work, it is clear that the only variables in (1) that can account for threshold voltage shifts are $\Delta\phi_b$ and Δd, since N_d, t_d, and ε are all fixed properties of a given heterostructure. Ideally, Δd is expected to be zero for a given heterostructure and gate recess etch depth; due to the extremely high selectivity of the wet-etch gate recess process used in this work, it is unlikely that any non-zero Δd values arise from gate recess processing. Using values for $\Delta\phi_b$ from diode measurements and threshold shifts of 108 mV for Ti/Au relative to Mo/Au and 381 mV for Pt/Au relative to Mo/Au results in inferred values for Δd of -17.5 Å and -47.8 Å, respectively, where the negative sign signifies that the gate appears to be closer to the channel for the Ti/Au and Pt/Au gated devices than for the Mo/Au reference devices. This reduction in effective gate-to-channel spacing is consistent with the observed trend in transconductance as well as threshold voltage; as shown in Table 2, the transconductance is lowest for the Mo/Au gate devices, larger for Ti/Au, and largest for Pt/Au, as would be expected if the gate were closer to the channel for Ti- and Pt-based gates.

Although transconductance is approximately inversely proportional to gate-to-channel spacing for very short gate lengths, the 0.7 μm gate lengths used in this work make analytical verification of the change in gate-to-channel spacing based on transconductance difficult. The long gate length also reduces the sensitivity of the output conductance to the gate-to-channel spacing; as shown in Table 2, the active-bias output conductance is virtually independent of gate metallization. From s-parameter measurements, however, the gate capacitance at pinchoff for pHEMTs with each gate metallization was extracted and compared. A simple series RC network was assumed as the equivalent circuit for the input of the pHEMTs at the onset of pinchoff, and gate capacitance computed from the imaginary part of z_{11}. Although this circuit model is an oversimplification for operation in the active region of device operation, at

TABLE 2
INGAP PHEMT PERFORMANCE PARAMETERS VS. GATE METALLIZATION

Gate Metallization	Peak Transconductance (mS/mm)	Output Conductance (mS/mm)	Threshold Voltage (V)	Unity Current Gain Frequency, f_t (GHz)	Max. Frequency of Oscillation, f_{max} (GHz)
Mo/Au	333	19.96	-0.694	41.3	101.1
Ti/Au	396	19.3	-0.586	38.8	93.8
Pt/Au	420	19.66	-0.313	36.0	73.0

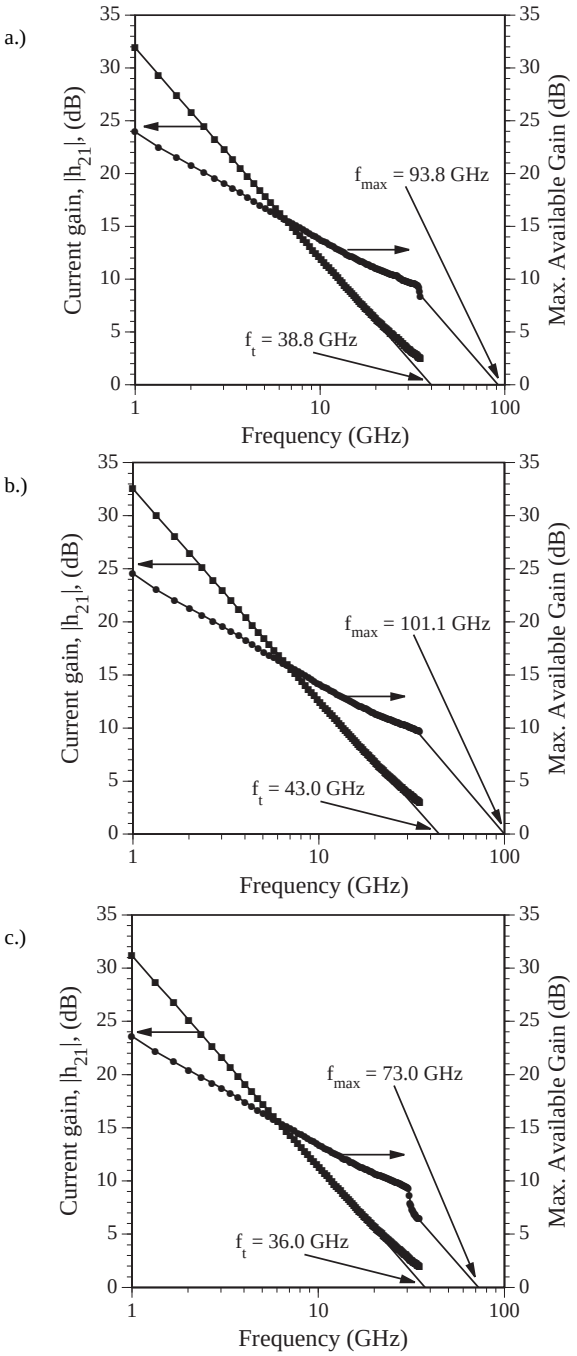

Figure 5. Microwave performance of 0.7 μm gate length pHEMTs fabricated with (a) Ti/Au gates, (b) Mo/Au gates, and (c) Pt/Au gates.

pinchoff where the transconductance and drain current are very small the error arising from source resistance feedback is negligible. Measurements of contact pad layouts yielded parasitic capacitances of 34 fF for the particular layout used for these pHEMTs; this capacitance was subtracted from the value obtained from s-parameter measurement of the pHEMTs to yield the intrinsic gate capacitance. The ratio of measured intrinsic gate capacitance for pHEMTs with each gate metallization relative to Mo/Au devices was computed, and is summarized in Table 3. In addition, the capacitance ratio that would be expected from the reduced gate-to-channel spacings as calculated from the shift in the threshold voltage is also included in Table 3. As can be seen, the change in gate capacitance that was observed matches closely the prediction based on a decrease in gate-to-channel spacing of 17.5 Å between Ti/Au and Mo/Au and 47.8 Å between Pt/Au and Mo/Au, with gate capacitance ratios of 1.056 and 1.207 measured and 1.062 and 1.19 obtained from predictions for Ti/Au and Pt/Au gates, respectively.

TABLE 3
RELATIVE MAGNITUDE OF INTRINSIC GATE CAPACITANCE VS. GATE METALLIZATION

Method	Mo/Au	Ti/Au	Pt/Au
Measured	1	1.056	1.207
Predicted from Δd	1	1.062	1.19

This reduction in effective gate-to-channel distance manifests itself in the microwave performance of the devices as well, as can be seen in the f_t and f_{max} performance summary included in Table 2. The steady decrease of both f_t and f_{max} with decreasing effective gate-to-channel spacing can be understood by noting that the gate capacitance is inversely proportional to gate-to-channel spacing, but the transconductance does not rise rapidly enough to preserve the g_m/C_{gs} ratio due to the relatively long gate lengths used in this study. Deep submicron gate length devices would not be expected to suffer from this speed penalty so acutely.

CONCLUSIONS

A study of Schottky barrier height and pHEMT performance for Mo/Au, Ti/Au, and Pt/Au gate metallizations was undertaken. A larger-than-expected shift in pHEMT threshold voltage for the different gate metallizations is explained in terms of a reduced effective gate-to-channel spacing for Ti/Au and Pt/Au gate contacts relative to Mo/Au contacts that is consistent with both dc and microwave measurements.

ACKNOWLEDGMENTS

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