Improved Manufacturability Methods for a High Volume, PHEMT Based, Ku-Band Power Module for VSAT Applications.

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Abstract

In order to manufacture a MMIC based module the manufacturer must have the ability to clearly identify final performance goals, establish a methodology to obtain these goals, and then fully integrate all aspects of the modules fabrication to produce a cost effective solution. This paper presents one approach used to develop a high volume, Ku-band module for VSAT applications. This 0.5 to 1 W module is designed around a four stage, 50 Ohm in/out PHEMT MMIC amplifier fabricated on Raytheon's 0.25μm T-gate process. By taking into account module and MMIC statistical distributions, providing wide spec margins at both MMIC and module production testing, and using a "design for worst case" approach, final MMIC yields of greater than 75% and final module yields greater than 85% are obtained. The use of an on chip resistive biasing network, coupled with simple DC sorting, allows a simplified off-shore assembly procedure which does not require individual module bias adjustments known to be typical for PHEMT based products. Further cost reductions are obtained through the use of a two step assembly procedure utilizing eutectic die attach and an epoxy attached substrate as well as high speed HP84000 testing at Ku-band.

Introduction

Based on end user specifications, the goal of this work was to produce a Ku-band module capable of a fixed output power between 0.5 and 1 W independent of input drive level. The module had to tolerate input drive levels varying over a 10db range as well as having relatively steep skirts for out-of-band rejection. Further, the module had to be unconditionally stable over all input drive levels and over a temperature range of -40°C to 75°C. In order to be cost effective, the MMIC itself was to be on-wafer RF probed for increased final module yield, and the module was to be assembled off-shore using a minimal parts count and minimal complexity. Final testing was to be performed at Raytheon, at Ku-band, using a high speed HP84000 tester.

Design Phase

In order to achieve a fixed output power independent of input drive level, the MMIC was designed with sufficient gain to drive the output stage well into compression even at the lowest input drive level encountered. To achieve this gain, a four stage amplifier was designed which produced the required gain with margin, matched to 50Ω at both input and outptut. The 50Ω in/out approach also had the advantage of improved on wafer RF testing while minimizing final assembly complexity and module parts count, thus reducing the overall module cost.

To produce both high on-wafer yield and module yield, variations in required gate bias were addressed using a on-chip voltage divider network. This network, shown in Figure 1, utilizes mesa resistors and allows the MMIC's quiescent current to be controlled using a fixed supply voltage and a unique wire bond configuration. On wafer RF probing utilizes pads 1 and 7 of Figure 1, with pad 1 connected to a fixed –5.0V and pad 7 connected to ground, to determine a reference quiescent current. Based on this initial measurement, those die falling outside the resistive network's range are inked out. An algorithm is used to match the reference current with a unique wire bond configuration which when applied, divides the –5.0V fixed bias supply to the appropriate gate bias to set the "proper" quiescent current. Although initially envisioned to be used to bin the die prior to shipping, it was determined that it was more cost effective to have the binning performed after module assembly and have an additional wire bond added to ground (i.e. to the appropriate pin 2 thru 6 of Figure 1) in order to achieve the final correct MMIC current. This method allows for a range of over 400mA of on-wafer-determined quiescent current to be compensated for in a simple and cost effective manner .

This module was expected to be a direct form, fit and

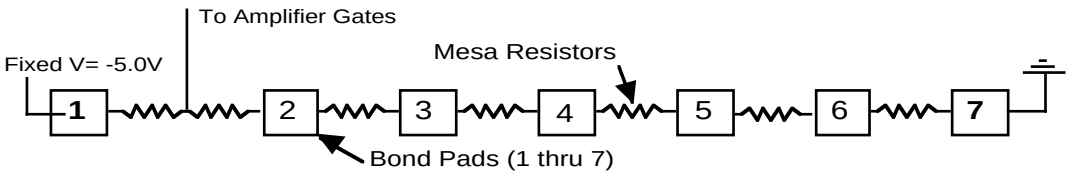

Figure 1: On chip resistor network used to bias all MMIC stages.

function replacement for an existing part, so the choice of module package was customer selected. Because of this, during the initial design phase, great care was taken to duplicate the final module environment as closely as possible in order to not only establish proper on-wafer MMIC specifications, but also to address stability issues early on. Initial designs were extensively checked for stability using the method of Normalized Determinant Functions (NDF)[1-3]. Further, given that at Ku-band package isolation is critical and the package itself was customer selected, MMIC input and output return loss was determined to be a critical factor affecting overall stability. This can be shown in equation (1) which relates the stability K-factor to small signal s-parameters.

$$K \approx \frac{\left(1-|S_{11}|^2\right)\left(1-|S_{22}|^2\right)}{2|S_{12}\|S_{21}|} \qquad (1)$$

Because S21 is the required gain and S12 is difficult to modify through design, S11 and S22 become the critical design factors in maintaining overall module stability

The MIMICs themselves were fabricated on Raytheon's 0.25µm PHEMT process. This process utilizes an optically-defined first recess and a tri-layer co-polymer resist stack with a single e-beam write step to define the second recess and T-gate. This process also utilizes full backside processing with through-wafer ground vias for improved device performance.

Figure 2 shows fixtured S21 and K measurements of the final MMIC amplifier at room temperature. As shown, even with these high gain devices the unconditionaly stable requirement is met as well as the relatively steep gain roll-off out of band.

Figure 3 illustrates the method used to establish the correct quiescent operating current. As seen in the figure, all currents used will produce a relatively flat saturated output power. However, the requirement of a fixed output power independent of input power determines a minimum Id value. For example, if a minimum input power of 5dBm is assumed an Id of at least 246mA must be established. This is a critical parameter relating to overall product yield because this Id value determines the range and resolution of the on-chip bias network as well as the absolute maximum and minimum values of the on-wafer Id screening limits. It was found that the correct resistive divider bias circuit was essential in achieving module yields in excess of 85%.

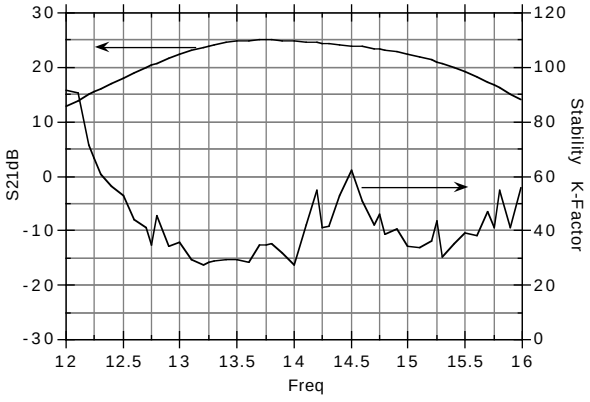

Figure 2: S21 and Stability K-factor versus frequency.

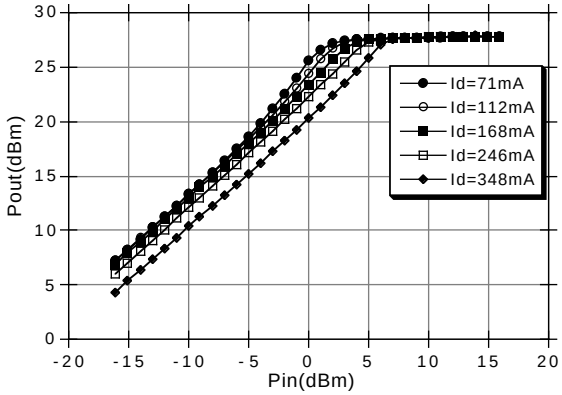

Figure 3: Pout versus Pin as a function of Ids.

Plots such as Figure 3, as well as similar plots at fixed Id and varying temperatures, were also used to establish the initial minimum on-wafer gain specs. In keeping with a "design for worst case" philosophy, all temperature testing was performed over the temperature range of -40°C to 90°C even though the final module specification range was from -40°C to 75°C. This was done to insure unconditional stability at the highest required temperature.

Production Phase

By utilizing a 50Ω in/out MMIC amplifier design, the final module parts count was kept to a minimum. In fact, only three external capacitors are needed in the final module as shown in Figure 4. In order to reduce final costs it was decided to assemble the module and perform DC bias testing

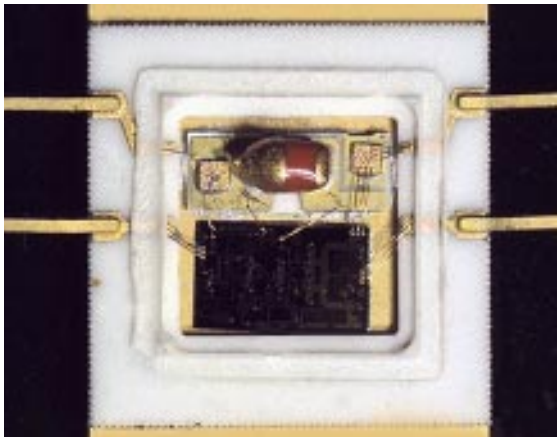

Figure 4: De-lidded Ku-band module.

off-shore. Final RF testing is performed using Raytheon's high speed HP84000 test bed operating at Ku-band with a total test time of 8 seconds/module.

Once the ramp-up to high volume production began, it was essential to have the ability to adapt quickly to any unforseen circumstances. At Raytheon, all process control data, DC and RF on wafer test data, and HP84000 module data is stored in an ORACLE data base. This allows for virtually instant evaluation of pertinent parameters in order to quickly identify problems, establish correlations, and modify on-wafer screening parameters to minimize final module cost and keep the volume of at-risk inventory small. The use of this database driven methodology is illustrated by a problem observed in one lot of wafers during the initial high volume ramp-up.

In order to insure output power flatness, a measurement of the difference between maximum output power and output power at a minimal input drive level is made during final RF module testing. Although initial low volume fixture measurements suggested an on-wafer gain of 24dB would produce acceptable module power flatness, a single lot was observed to produce only a 20% module yield as opposed to the more typical 80% module yield. In an attempt to determine the cause, a plot was made of change in output power versus on wafer RF gain. This analysis, shown in Figure 5, clearly shows that for this lot, a 26 dB on-wafer gain spec would have given a power output change of less than 0.25 dB over all input power levels. Once this module to wafer-level correlation was established, on wafer RF data was analyzed to establish the potential effects this 26 dB minimum gain spec would have on on-wafer yield. Figure 6 shows a histogram of S21 for over 12,000 die with the highlighted portion indicating those die with S21 < 26 dB. This shows that a 26 dB gain spec on-wafer would have minimal impact on overall wafer yield.

Final module yield was also used to fine tune the minimum and maximum drain current specification used during the on-wafer RF measurements. It was found that in order for the on-chip resistor divider network and its associated wire bond algorithm to work correctly, Id had to vary linearly with gate bias. This linearity requirement set the minimum acceptable Id value, while the range of the resistor divider circuit set the maximum Id value. Once these minimum and maximum Id values were determined, DC bias yield of modules measured off-shore was seen to be over 90%. The use of the modified S21 specification also caused final RF module yield to increase to over 90%.

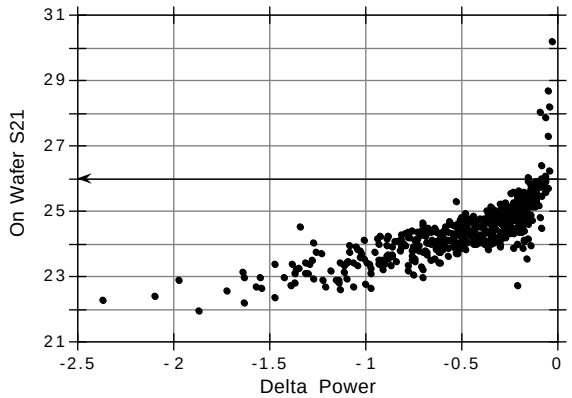

Figure 5: Power flatness versus on-wafer gain.

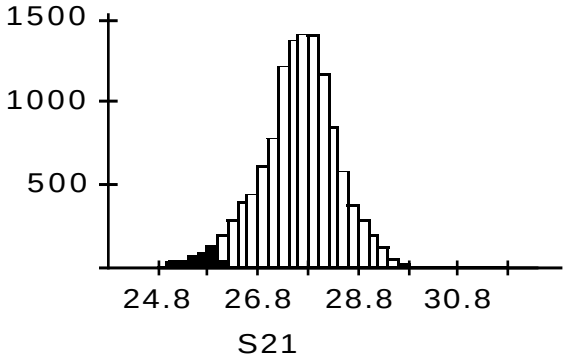

Figure 6: On wafer gain histogram. Highlighted region has gain < 26dB.

Conclusion

Through the use of an integrated design philosophy, along with real time, high volume data analysis, final on-wafer yields of 75% and final module yields in excess of 85% are achievable for high end, high volume modules operating at Ku-band. This work describes a method that can be used to address known variations associated with a PHEMT's required gate bias through the use of an on-chip resistor network and a simple assembly procedure. It is also shown that by adopting a "design for worst case" approach, unconditional stability can be achieved for even high gain modules by addressing both MMIC design and package issues early in the design phase. The use of integrated database management is also shown to be essential for a quick response to unforseen performance variations observed during the initial high volume ramp-up.

References

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