A GaAs Fab's Approach to Design for Manufacturability

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ABSTRACT

Too often in manufacturing, one finds products which do not yield over all processes. Product engineering, test, design and wafer fabrication groups work after the fact to resolve yield issues. Products are redesigned, process windows changed or specification relief is asked for in an attempt to make up lack of proactive engineering. Through proactive engineering, products could be designed for manufacturability.

Another difficulty in design is the difference between DC tests parameters from the fab and RF results that must be taken into account in the design. MMIC devices are unique in the fact that RF parameters are required of them in all applications. At the same time, it is costly and difficult to perform 100% RF testing at the wafer level. It is much more efficient to perform DC tests as historically done in Silicon processing. DC tests can be done in two ways, i.e., Process Control Monitoring (PCM) and Unit Test whereby each product die is tested with a unique and usually shortened test scenario.

In order to help in the overall yield improvement, the fab can do several things to improve the manufacturability of a device. Through implant control and induced epitaxial variation, the process window can be artificially induced on a first lot. Evaluation of this device can result in correlation between PCM, Unit Test and final RF test at the package level. Test capability and system variation can be taken into account. We call this the process corners method.

In this paper, we will describe this method for correlation of DC tests to final RF tests. Using this method, correlations greater than r^2=0.8 have been achieved. It is our contention that having such correlation allows the exemption of on-wafer RF testing. Furthermore, it will be shown that once specification limits are set using a dose split of process corners method, yield results at PCM and Unit Test track quite well with final RF tests done on packaged parts. Moreover, data from the process corners method can be used to generate design rules that take into account the process capability of the fab. We will discuss the fab's contribution to improvements in design and testing for manufacturability as well as similar results for variation in heteroepitaxial material.

INTRODUCTION

With the increased demand for GaAs MMIC devices, comes a need to become more efficient in the production of such devices. One way to increase the efficiency of any manufacturing process is by eliminating steps. Yet another method is to design for manufacturability. In this paper, we describe a method for elimination of on-wafer RF testing. This is done by the process corners method whereby an implantation dose split is done across the specification window and the parts tested at a process control monitor (PCM) and a DC test on individual units (Unit Probe). Final RF testing data is then correlated to Unit and PCM data. This provides an opportunity to eliminate on-wafer RF testing. Furthermore, it allows feedback to the designer as to how the devices perform across the process window.

EXPERIMENTATION

One lot of MMIC Power Amplifier devices was processed under normal conditions with the exception of the ion implantation dose. The implantation dose was varied ±15% from normal. Here normal means the nominal implantation dose that is normally used for

devices having similar processes. The dose split yielded a current (Idss) split, which is shown in Fig. 1.

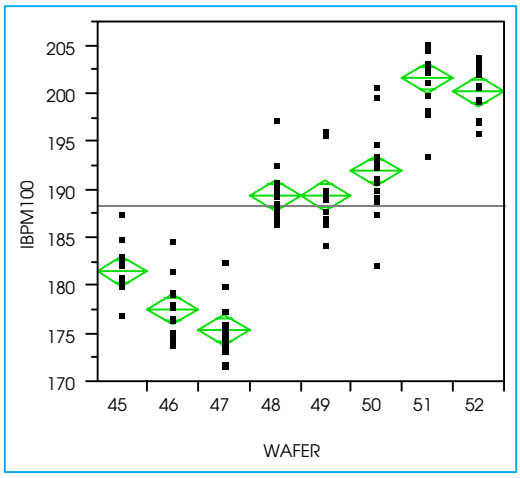

Figure 1- Dose split across the process spec window. Here wafers were implanted with a separate dose to induce a current (Idss) split on power FETs.

In a power amplifier of this type, characterization of only one FET is necessary. It is important to split all the FETs that constitute the MMIC device. This way the entire device is characterized over the range of interest. In this figure one can see that each current split is linear across the lot which is expected given the dependence of current on channel charge[1]. In other MMIC devices such as a low noise amplifier (LNA), for example, the depletion and enhancement FETs must be split in this manner. These are shown in figs. 2-3. In fact, the dat given here indicated the splits were ±10% as well as ±15%. Thus, making sure the splits runs across the target and the spec limits of the device.

It should be noted that parametrics from other PCM structures were compared to the baseline or historical values to assure that the lot was processed without aberration. These PCM structures include sheet resistance, contact resistance, gate length, gate metal sheet resistance and breakdown.

Although this device is a power amp, the current splits shown in fig. 1 are of individual FETs on the PCM structure. This PCM structure is on every reticle and is repeated approximately sixteen times to give that many data points in the data shown. The means diamonds in these figures represent the quartile of the spread in the data. The center of the diamond is the mean value for that wafer.

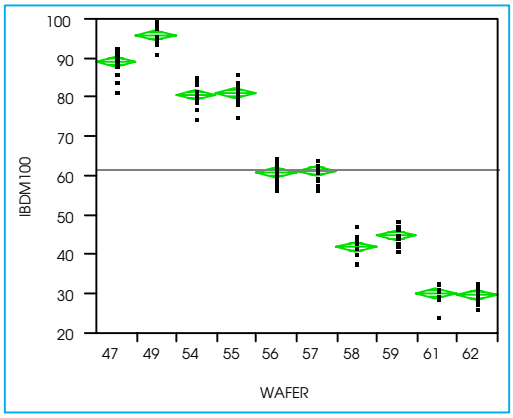

Figure 2- Dose split across the process spec window. Here wafers were implanted with a separate dose to induce a current (Idss) split on depletion FETs.

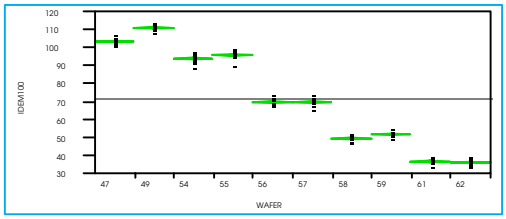

Figure 3- Dose split across the process spec window. Here wafers were implanted with a separate dose to induce a current (Idss) split on enhancement FETs.

It should be noted that these current splits fall slightly above the specification limits for these devices. The reader should be aware that in repeating this experiment in his/her fab, the implantation dose splits should vary across the specification window and not arbitrarily be split ±15% from normal. This specification window may be larger or in many cases tighter than the example given here. The comparison with baseline data is imperative since changes in an uncharacterized process is another source of error in this method.

After electrical test and characterization at PCM the lot was DC tested at Unit Probe. At this stage of the process, a unique measurement is made for a particular MMIC device. For example, in a low noise amplifier, where depletion and enhancements FETs are used, the total current of the device would be a sufficient test for Unit Probing so

long as the grounded parts had a capacitance to avoid leakage. On the other hand, in the case of an upconverter the minimum current while the part is enabled and a maximum current when the part is disabled could serve as a good measure of the device as a whole.

In this case, a power amplifier is used as a dual band driver for cellular phones. This device has two stages and the threshold voltage as well as the quiescent current is measured for both stages.

After Unit Probe, the individual dice were packaged and RF tested. This is called Final Test. The details of Final Test will not be covered here except to state that the output current and gain are the two most important parameters.

RESULTS

The correlation between Unit Probe and PCM exists. This is shown in fig. 4. In this plot, the threshold voltage of the first stage at Unit Probe is given as a function of the threshold voltage of the power FETs at the PCM locations. Here the correlation is statistically signifigcant (r^2=0.994). [2]

Since the maximum power gain of a MESFET amplifier is linearly proportional to the current, a direct linear correlation of the maximum power out and the threshold voltage is expected.[3] This is shown in fig. 5.

Here the output power set at maximum gain is plotted versus the second stage threshold voltage, Vth_2. Note that the correlation is also statistically significant (r^2=0.9).

This allows the generation of DC specification limits based on RF parameters.

Furthermore, based on this data and based on historical data the designer now has a feel for how devices will operate over the GaAs fab's operating range or the PCM specification window.

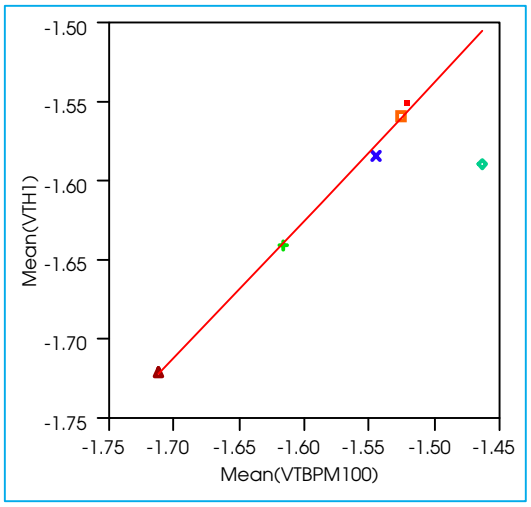

Figure 4- Threshold voltage of the individual power FETs correlated to the DC threshold voltage measured at unit probe. R^2=0.994

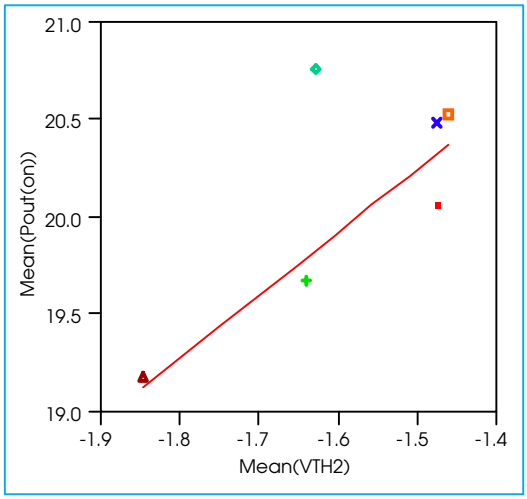

Figure 5- Output power in RF correlated to the DC threshold voltage measured at unit probe. R^2=0.9

DISCUSSION

The purpose of this study was two-fold. The primary purpose was to correlate Final Test to Unit Probe and PCM. This saves time and reduces cost since electrically out-of-spec wafers do not go on to Unit Probe and failed Unit Probe dice do not go on to Final Test. The fallout, therefore, at Final Test should be in the low 1-3% range. This is a tremendous saving as compared to sending all dice to get packaged and RF tested. This may not be a common practice, anyway. However, even on-wafer RF

testing is expensive. This method eliminates the equipment and expertise needed for on-wafer RF testing.

The secondary purpose, and yet just and important, was to provide designers the process corners of the FETs used in the MMIC devices. When a particular parametric value is used instead of a more realistic range, it becomes possible for the device to fail without detection by PCM or Unit Probe. This is where the fab can contribute to the design and thus have a true design for manufacturability. This is especially true for GaAs fabs where the modeling of devices is lacking to their sister fabs in the silicon world.

Undoubtedly, the key to successful correlations is to select a Unit Test that is meaningful. The test should examine the critical parts of the circuit and yet be fundamental enough so as to correlate with the single FETs of PCM. Once this test is established, the process corners experiment described herein can be accomplished.

CONCLUSION

In this study, the authors have shown a correlation among PCM, Unit Test and Final Test can be accomplished. This is done by performing a dose split across the specification window of the process. This is called a process corners experiment. The process corners experiment, if done properly, can provide DC test specifications, which correlate with Final RF testing. This can be used in lieu of on-wafer RF testing which is expensive. Furthermore, feedback to the designers on the performance of the devices across the process range can be used to enhance their designs. This is what is considered the fab's contribution to design for manufacturability.

REFERENCES

1. Liao, S.Y., Microwave Devices and Circuits, Prentice Hall, Englewood Cliffs, N.J. 1980 P.296.

2. Ott, L., Statistical Methods and Data Analysis, PWS-Kent, Boston, 1988 P. 319.

3. Sze, S.M., Semiconductor Devices, Physics and Technology, John Wiley and Sons, N.Y. 1985 P. 183