Advanced InP/InGaAs HBTs Technology for Low-Power Lightwave Communication Circuit Applications (Invited)

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ABSTRACT

A reliable non-self-aligned process technology has been developed for InP/InGaAs HBTs with a carbon-doped base and applied to 40 Gbit/s lightwave communication ICs. A hexagonal shaped emitter geometry aligned parallel to the Primary Flat of wafer is used to suppress the periphery base leakage current originating from the side-wall of the InP emitter-mesa. This emitter orientation leads to stable emitter/base-junction I-V characteristics. In addition, a dehydrogenation annealing method was devised to activate the carbon acceptors of the InGaAs base layer, which is passivated by hydrogen during MOVPE growth. A 6-μm^2 hexagonal emitter HBT with a 1.2 μm width showed peak f_T of 135.8 GHz and f_{max} of 183.7 GHz. A 40-Gbit/s 1:4 demultiplexer IC, a 40-Gbit/s decision IC, and a 40 GHz static 2:1 frequency divider IC were fabricated using non-self-aligned InP/InGaAs HBTs. The power dissipations of the 1:4 demultiplexer and decision ICs were as low as 2.97 and 0.94 W, respectively.

INTRODUCTION

InP-based HBTs using InGaAs as a base have a number of advantages when compared with GaAs-based HBTs, such as ultra high speed, low turn-on voltage, and direct compatibility with lasers and pin diode photodetectors for 1.3-μm radiation. These advantages make the InP-based HBT an attractive candidate for use in large-capacity lightwave communication systems for future multimedia services. There has been remarkable progress recently in the development of InP-based HBTs for over 40-GHz static frequency dividers [1-3]. In particular, M. Sokolich, et al. have demonstrated that their InP HBTs with a maximum clock speed of 53 GHz are superior to SiGe HBTs in terms of power dissipation. They suggested that their InP HBT production level will enable multiplexer and demultiplexer circuits to operate at 100-Gbit/s [3]. However, a refined self-aligned process approach has been often used for high-performance HBTs. On the other hand, a simple non-self-aligned process depending on conventional lithography promises reproducibility and uniformity across the wafer for MSI-LSI technology.

In this paper, we describe an advanced device technology of non-self-aligned InP/InGaAs HBTs for 40-Gbit/s class ICs. The outstanding feature of our InP/InGaAs HBT is the hexagonal shaped emitter geometry aligned parallel to the Primary Flat of wafer. Only this crystallographic facet (near (111)A) of the InP emitter mesa provides stable emitter/base junction I-V characteristics because unfavorable periphery base leakage current is well suppressed. Bias-stress tests revealed little change in the current gain even after 2448 hours at a collector current density (J_C) of 60 kA/cm^2 under an ambient temperature of 180° C [4]. Furthermore, a carbon (C)-doped InGaAs base layer is used to reduce dopant diffusion.

DEVICE FABRICATION TECHNOLOGY

The HBT layer structure used in this study was grown by low-pressure metalorganic vapor phase epitaxy (MOVPE) on a 3-inch semi-insulating (100) InP substrate. In MOVPE-grown HBTs, a serious problem is that hydrogen makes the C acceptors in the InGaAs base layer inactive during growth. The sheet resistance of the as-grown C-doped InGaAs layer (50-nm) is very high (6250 Ω/sq.). A good way to reactivate the C acceptors is to reduce the amount of H by high-temperature annealing. However, conventional annealing, which is carried out on an as-grown HBT wafer, does not sufficiently reactivate the C acceptors because the n-type emitter layers capping the base region act as a barrier to the out-diffusion of hydrogen atoms due to the built-in electric field in the depletion region [5]. We, recently, devised a new method of dehydrogenation annealing. The annealing is performed after emitter-mesa formation, that is, after the C-doped InGaAs layer is exposed. This allows the H atoms to escape directly from the surface of the layer [6].

Our standard HBTs start with InGaAs/InP emitter mesa formation by means of ECR-RIE and selective wet etching. After high-temperature dehydrogenation annealing, the base electrode

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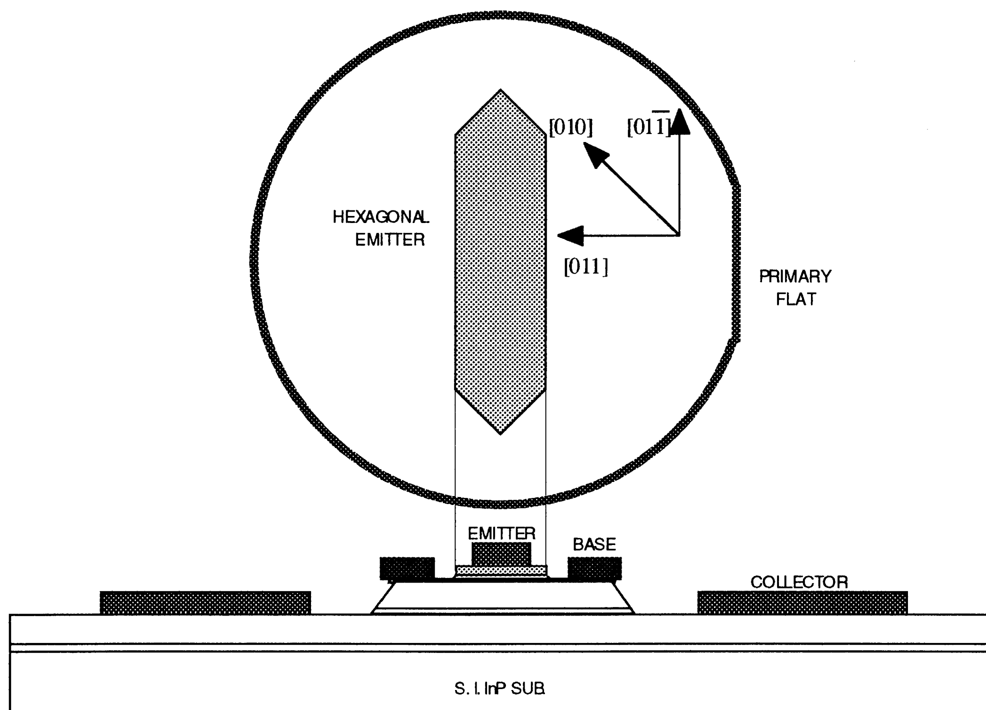

Fig. 1. Schematic cross-sectional view of InP/InGaAs HBT.

metal is evaporated in a non-self-aligned manner. Then, a composite collector layer structure consisting of undoped InGaAs and n-doped InP is removed by selective wet-etching, and the emitter and collector electrode metals are formed by evaporation and a lift-off technique. Figure 1 shows a schematic cross section of our InP/InGaAs HBT with its hexagonal emitter shape. Benzocyclobutene (BCB) films are used for the device passivation.

DEVICE CHARACTERISTICS

Figure 2 shows the typical common-emitter/collector I-V characteristics for a 6-μm^2 emitter HBT with an emitter width of 1.2-μm. We produced two HBT wafers with identical layer structure and fabrication process (wafers #1 and #2). The current gains at a J_C of 30 kA/cm^2 were 33.7±4.4 and 35.2±3.8 for wafers #1 and #2, respectively. The extrinsic base resistance was estimated simultaneously using a TLM method. The sheet resistance and specific contact resistance were 595±29 Ω/sq. and 0.14±0.02 μΩ-cm^2, and 602±31 Ω/sq. and 0.14±0.02 μΩ-cm^2 for wafers #1 and #2, respectively. These results indicate that our dehydrogenation annealing achieves both uniform and reduced base resistance, R_B, without any current gain reduction. The R_Bs of a 6-μm^2 emitter HBT were approximately 34.7 and 35.1 Ω for wafers #1 and #2, respectively.

The high-frequency characteristics of non-self-aligned HBTs

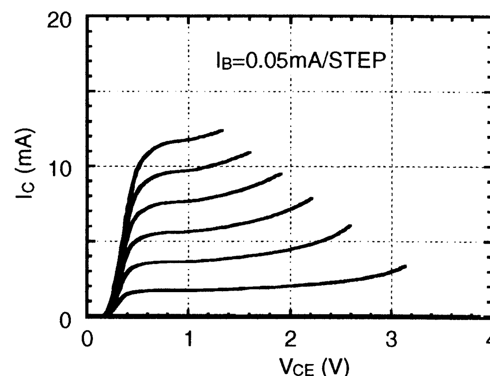

Fig. 2. Typical I_C-V_{CE} characteristics of 6-μm^2 emitter HBT

strongly depend on the spacing between the InP emitter-mesa and the base metal. Thus, we examined the dependencies of f_T and f_{max} on this emitter/base distance, D_{EB}, for a 6-μm^2 emitter HBT. The f_Ts were almost constant, while the f_{max}s increased as the D_{EB} became shorter due to a reduction of parasitic R_B and C_{BC}. In our standard HBT process, a 0.3 μm spacing is used as D_{EB} in view of the transistor yield. Figure 3 shows the dependencies of the estimated f_T and f_{max} on I_C at a V_{CE} of 1.3 V for wafer #1 with a 6-μm^2 emitter HBT. The dependencies of f_T and f_{max} on V_{CE} at an I_C of 4 mA are shown in Fig. 4. The peak f_T and f_{max} were 135.8 and 183.7 GHz,

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respectively. This f_{max} is high due to the optimum dehydrogenation annealing in spite of the non-self-aligned HBT. Across the wafer, f_T and f_{max} were 115.5±7.5 and 165.2±19.4 GHz, and 116.4±4.4 and 169.3±4.2 GHz at a J_C of 50 kA/cm^2 for wafers #1 and #2, respectively. The non-self-aligned process approach improved the reproducibility and uniformity of the device characteristics.

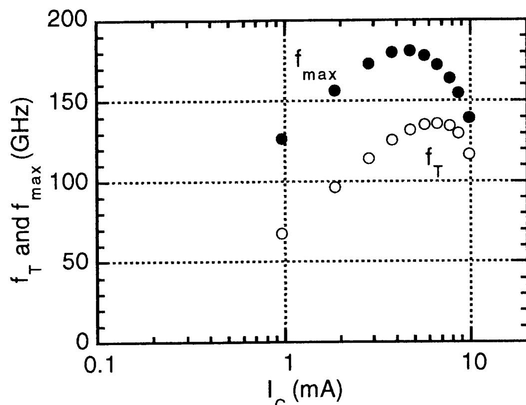

Fig. 3. f_T and f_{max} dependencies on I_C for 6-μm^2 emitter HBT.

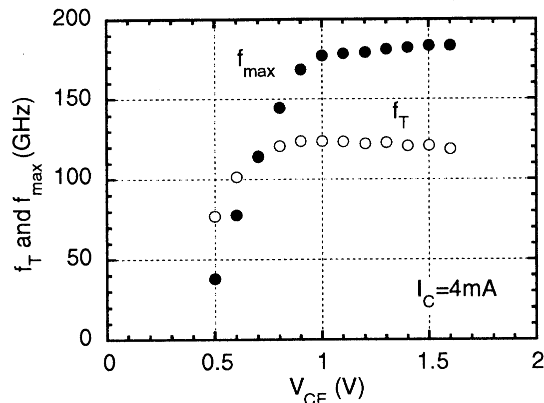

Fig. 4. f_T and f_{max} dependencies on V_{CE} for 6-μm^2 emitter HBT.

IC PERFORMANCE

We fabricated 19-stage emitter-coupled logic (ECL) series-gate ring oscillators to assess the uniformity of the circuit performance. Each ECL gate contained seven HBTs. Figure 5 shows a histogram of the propagation delay for wafer #1. We obtained a low propagation delay per gate (6.85 ps), and a very small standard deviation (0.078 ps), corresponding to just 1.1%. This good uniformity of the ring oscillator performance is attributable to our non-self-aligned HBT process technology.

We confirmed 40-Gbit/s operation in a decision IC fabricated using our 6-μm^2 emitter HBTs [7]. Power dissipation was 0.94 W at a supply voltage of –4.5 V, which is about half that of the InP-based HEMT decision IC. Moreover, a 40-Gbit/s demultiplexer IC was fabricated using the 6-μm^2 emitter HBTs with an f_T of 115 GHz and an f_{max} of 154 GHz [8]. Its power dissipation was 2.97 W at a supply voltage of –4.5 V. Reducing the current in the 2:4 DEMUX part will further reduce consumption.

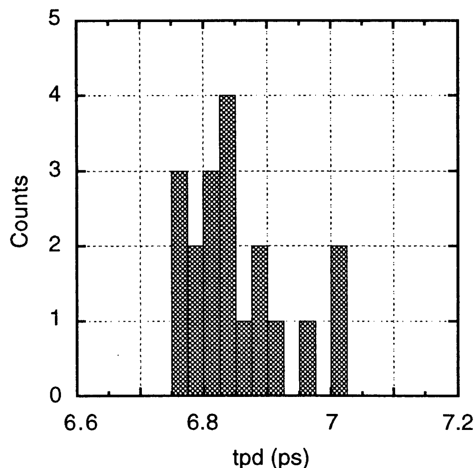

Fig. 5. Propagation delay for ECL 19-stage ring oscillator.

We also fabricated a static 2:1 frequency divider IC with a 900 mV logic swing consisting of a master-slave ECL T-FF and input/output buffer and a static 32:1 frequency divider IC consisting of five-stages T-FFs and input/output buffers [9]. The maximum operating frequencies were 40-GHz for the T-FF and 35-GHz for the 32:1 divider. The first-stage T-FF, identical to a 2:1 divider, dissipated 186.8 mW, and the T-FFs for the gates in the second and following stages dissipated only 63 mW. These results show the feasibility of using non-self-aligned InP/InGaAs HBTs for high-speed low-power IC applications.

To confirm the low-power advantage offered by InP/InGaAs HBTs, we fabricated two kinds of static 4:1 frequency dividers consisting of either two ECL or two current-mode logic (CML) T-FFs and an output buffer. The ECL divider operated at up to 39.7-GHz and dissipated 120 mW per flip-flop. The maximum frequency of the CML divider was lower (31.5-GHz), but the flip-flops dissipated an extremely low power (32 mW). Figure 6 compares the reported maximum operating frequencies against the power dissipation per flip-flop for InP- and GaAs-based HBTs and InP HEMT. The InP-based HBTs, including the ones we made,

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dissipated much less power than the GaAs-based HBTs.

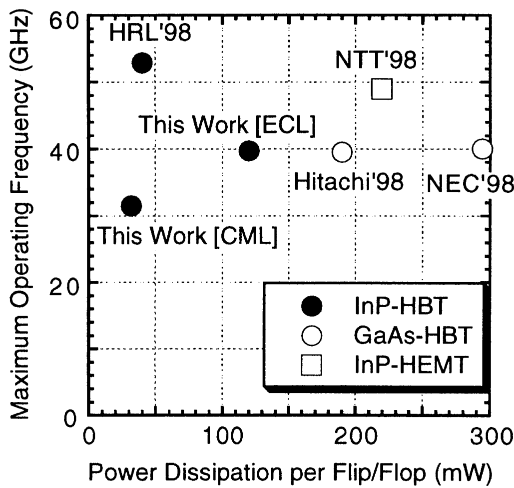

Fig. 6. Comparison of flip-flop power dissipation between InP- and GaAs-based HBTs and InP-HEMT.

CONCLUSION

We have developed non-self-aligned MOVPE-grown C-doped InP/InGaAs HBTs with a hexagonal emitter aligned parallel to the Primary Flat of wafer. This unique emitter-mesa geometry provides highly reliable emitter/base-junction I-V characteristics. Although an inactive acceptor in the C-doped InGaAs base layers due to hydrogenation prevented reducing in their base resistance, we overcame this problem by using a new high-temperature dehydrogenation annealing method, resulting in good high-frequency characteristics in spite of the non-self-aligned HBT. The 6-μm² hexagonal emitter HBT with a 1.2 μm width showed a peak f_T of 135.8 GHz and f_{max} of 183.7 GHz. A 40-Gbit/s 1:4 demultiplexer IC, a 40-Gbit/s decision IC , and a 40 GHz static 2:1 frequency divider IC were fabricated using our non-self-aligned InP/InGaAs HBTs. The power dissipations of the 1:4 demultiplexer and decision ICs were as low as 2.97 and 0.94 W, respectively.

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