RF-LDMOS: A Silicon-Based, High Power, High Efficiency Linear Power Amplifier Technology

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Abstract

RF-LDMOS is a leading device technology for high power, high efficiency linear RF power amplifiers. The versatility of this technology is highlighted in three applications: 1) a 28V, 220W P3dB push-pull device designed for Wideband CDMA; 2) a 26V, 10W RF-LDMOS multi-stage integrated power amplifier (IPA) for the 900MHz GSM market; and 3) a new 50V RF-LDMOS platform for the broadcast and cellular infrastructure markets. In addition to its excellent linearity and efficiency, the 220W transistor is, to our knowledge, the highest power Si device ever reported for the 2GHz cellular market.

INTRODUCTION

High power, high efficiency linear RF power amplifiers (PA's) are widely deployed in cellular base stations. The emerging high-definition television broadcast market requires similar high performance PA devices. With the advent of spread-spectrum modulation formats such as Wideband CDMA (WCDMA), system requirements demand dramatically improved linearity in addition to the ongoing progression towards higher power and higher efficiency PA's. While the market demands the highest performance level from the PA device manufacturer, there is also an expectation of unsurpassed reliability and lowest possible cost. The device manufacturer must navigate successfully within these oftentimes conflicting constraints to deliver winning solutions to the infrastructure markets.

RF-LDMOS (Laterally Diffused Metal Oxide Semiconductor) emerged during the 1990's as a leading RF PA device technology for infrastructure applications [1-3]. High power, efficiency, and linearity are the most well known attributes of this Si-based technology. The equipment manufacturer's cost goals are achieved by leveraging the extensive silicon manufacturing base, which yields low die fabrication costs, and the simple packaging afforded by the inherent backside source contact. Reliability expectations have also been met through careful device design and layout considerations.

This paper will present key details of the RF-LDMOS fabrication process. Reliability considerations will also be presented. Three applications will then be presented which illustrate the versatility of this device technology: 1) a 28V, 220W P3dB push-pull device designed for WCDMA; 2) a 26V, 10W RF-LDMOS multi-stage integrated power amplifier (IPA) for the GSM market; and 3) a new 50V RF-LDMOS platform designed for the very high power broadcast and cellular infrastructure markets. In addition to its excellent linearity and efficiency the 220W transistor is, to our knowledge, the highest power Si device ever reported for the 2GHz cellular market.

DEVICE FABRICATION

The RF-LDMOS transistor is essentially an MOS transistor optimized for RF power applications, ensuring compatibility with the large, established silicon MOS manufacturing base. A cross-section through a single finger of the transistor is shown in Fig. 1. The transistor is fabricated using p- epitaxy on p+ substrates. The epitaxial layer is lightly doped (10 Ω-cm) to reduce the output capacitance C_{DS} and increase the breakdown voltage BV_{DSS} (65V min. for 28V operation, 120V min for 50V operation). A deep p+ sinker diffusion links the n+ source diffusion to the p+ substrate, providing a simple implementation of a backside source. Typical gate lengths are 0.40-1.0μm, while gate oxide thicknesses vary between 400-700Å for operating voltages of 28-50V. The gate is formed by a polysilicon/WSi stack with a sheet resistance of 1Ω/sq to lower the gate access resistance R_G, ensuring compatibility with high frequency operation.

A key departure of the LDMOS structure from a typical VLSI/ULSI MOS structure is the asymmetrical fabrication of the device. The PHV implant on the source side of the device establishes the threshold voltage, turn-on behavior, and punchthrough characteristics of the device. The NHV region on the drain side determines the breakdown voltage and

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strongly influences the hot carrier injection (HCI) reliability of the device.

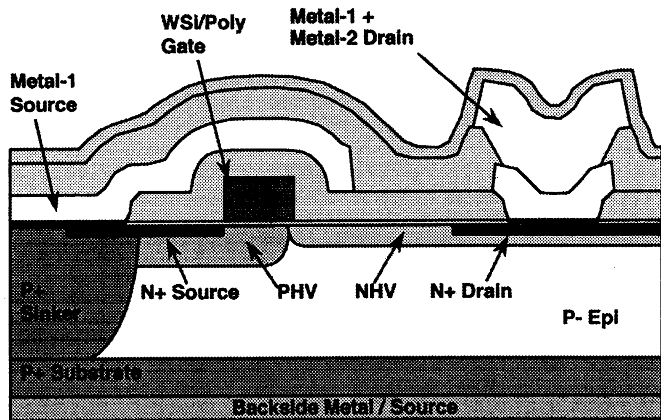

Fig. 1: Cross-section through a single finger of the RF-LDMOS transistor.

The source metal is used to both connect the n+ source diffusion to the p+ sinker, and to minimize the feedback capacitance C_{GD} between the gate and the drain metal by extending over the gate electrode to form what is termed a Faraday shield. The drain metal is formed using a two layer metal stack with a thick (3.6μm) 2nd metal to satisfy the electromigration requirements. An AlCuW alloy with excellent intrinsic electromigration characteristics is employed to ensure compatibility with advanced process equipment.

RELIABILITY CONSIDERATIONS

HCI effects are a key concern for all MOS transistors. The design of the NHV region is critical to suppress HCI without degrading the on-resistance (R_{DSON}) or BV_{DSS}. The most recent generations of Motorola's 26V platforms, known as HV4 and HV4x4, are capable of suppressing HCI effects to an Idq drift of ~5% in 20 years. The 50V platform also exhibits an Idq drift of less than 10% in 20 years under typical bias conditions.

The electromigration performance of the top metal is another key reliability consideration. Motorola's high voltage RF-LDMOS platforms incorporate a thick 2nd layer AlCuW metal on the drain region and feed structures to meet the design target of >100 years MTTF at 200°C junction temperature under rated RF operating conditions. Finally, although not generally available by other LDMOS manufacturers, ESD input protection to protect the ESD-sensitive gate oxide has been designed into Motorola's 50V platform, HV4/HV4x4 28V platforms, and the new 900MHz and broadcast market products. Typical performance is an ESD rating of >2000V Human Body Model (HBM). ESD ratings without the ESD circuitry would be in the 100V range.

DISCRETE DEVICE PERFORMANCE AT 28V, 2GHZ

Motorola's 4th generation 28V RF-LDMOS platform, HV4x4, features 0.60μm gate lengths, 400Å gate oxide, 65V minimum BVdss for excellent ruggedness, 4 mil die thickness for thermal management, and unsurpassed reliability (>100 year metal MTTF, input ESD protection, and Idq drift projected to be in the 4-6% range over 20 years). A 360mm single-ended HV4x4 device was recently reported [3] which delivers 155W (P_{3dB}) at 48% drain efficiency, measured at 2.12GHz, 28V, Class-AB bias (see Fig. 2).

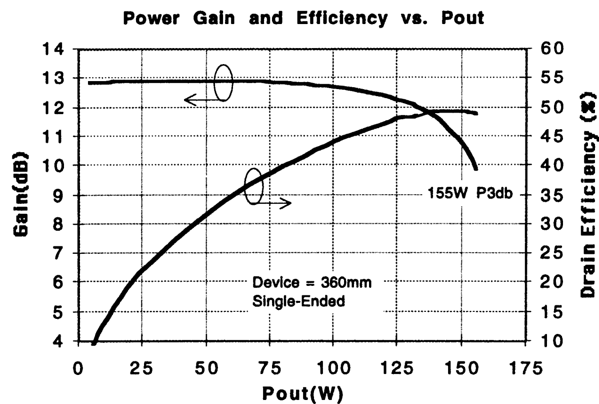

Fig. 2: Power gain and drain efficiency vs. output power for the 155W (P_{3dB}) single ended device operated at 2.12GHz, 28V.

An HV4x4 push-pull device has recently been developed that has a total gate periphery of 480mm. Fig. 3 plots the gain, drain efficiency, and output power as a function of input power under single-tone (2.12GHz) CW conditions at 28V, Class-AB bias. The device delivers 220W (P3db) at 46% efficiency.

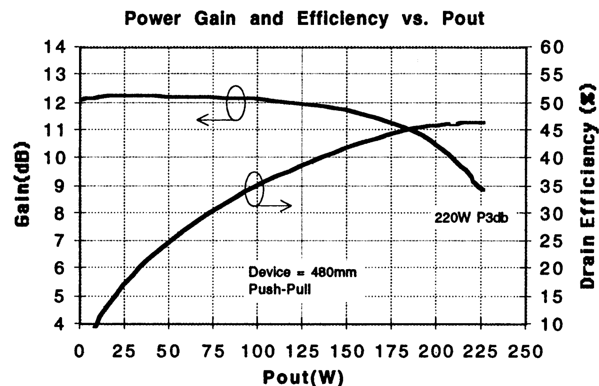

Fig. 3: Single tone output power, drain efficiency, and gain vs. Pin for the 220W (P_{3dB}) push-pull device operated at 2.12GHz, 28V.

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While high CW power levels at 2GHz are a significant accomplishment, the key distinguishing feature of RF-LDMOS is its superior linearity. Fig. 4 plots the two-tone third order intermodulation distortion (IMD3) vs. P_{OUT} (PEP, tone spacing of 10MHz) for a range of Idq settings for the 155W single-ended device.

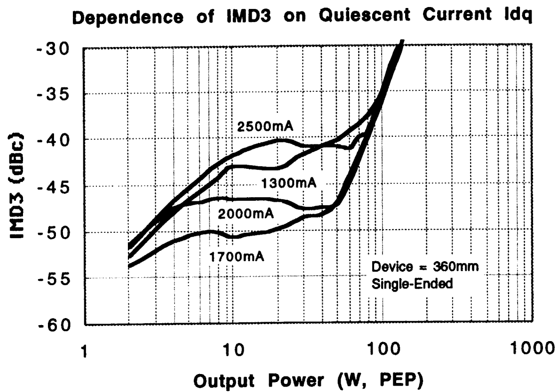

Fig. 4: Class-AB Two-Tone IMD3 vs. output power as a function of drain bias. The device is a 360mm single-ended design. The drain supply was 28V, with the frequency centered at 2.12GHz (10MHz tone spacing).

Note the outstanding backoff linearity at the optimum Idq setting. Well-designed RF-LDMOS transistors typically achieve IMD3's of -40dBc at 3dB backoff from the –30dBc two-tone rated power, and continue down to –50dBc in the 7-10dB backoff regime, without the pronounced backoff hump observed in many technologies. Along with good fifth and seventh order linearity, this outstanding backoff linearity improves PA performance for modulation formats with high peak-to-average ratios, including WCDMA.

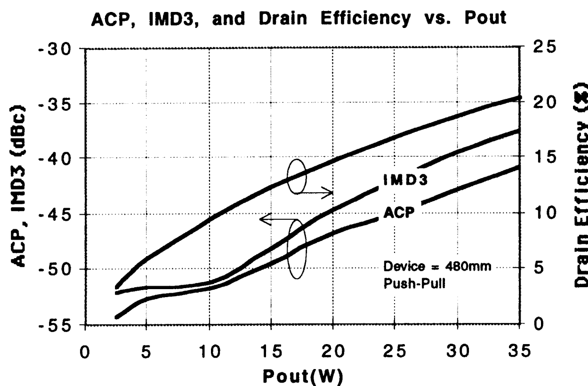

Fig. 5: Multi-carrier WCDMA plot of IMD3, ACP, and efficiency vs. output power. See the text for additional test conditions.

A different set of measurements must be taken to quantify the performance for WCDMA applications. A multi-carrier WCDMA amplifier has the most stringent linearity constraint. Linearity is measured by using two WCDMA stimuli (8.5dB peak to average ratio) with a spacing of 10MHz (f1=2.1125GHz, f2=2.1225GHz). IMD3 is then calculated by integrating the power in 3.84MHz bandwidths at 2.1335GHz (IMD3+) and 2.1025GHz (IMD3-). The average power achieved for the 480mm push-pull device at an IMD3+/- of –40dBc is about 30W with a drain efficiency of 19% (see Fig. 5).

INTEGRATED POWER AMPLIFIERS: A 3-STAGE IPA FOR GSM

Multi-stage Integrated Power Amplifiers (IPA's) have been made possible by integrating series and shunt capacitors, along with multi-level metal inductors and transmission lines into the RF-LDMOS flow [4]. The results reported here are based upon the IPA version of the HV4 discrete device flow, termed HV4IC. Fig. 6 presents the layout of a 2-stage IPA designed for 10W CW at 26V, 1GHz for the GSM market. This design integrates most of the input and interstage matching network.

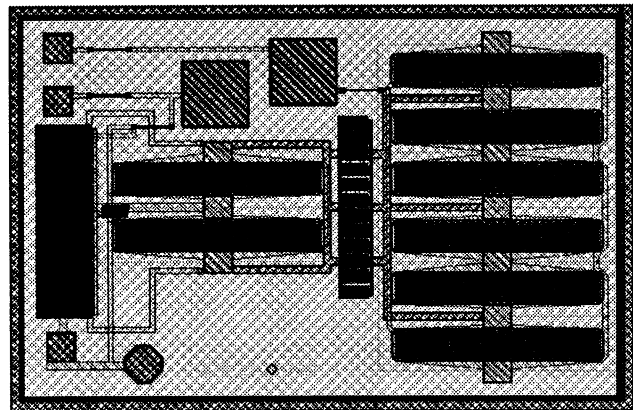

Fig. 6: Layout of a 2-stage IPA designed for 10W, 26V, and 1GHz.

Fig. 7 plots the gain and PAE vs. output power at 950MHz, 26V for an advanced 3-stage IPA with fully integrated input and interstage matching. The peak PAE is 52% at the 1dB compression point, which corresponds to an output power of 12.6W. The overall gain of this amplifier is 40dB. Motorola's RF-LDMOS IPA roadmap includes IPA's for the 1-2 GHz market in support of all major cellular bands. In addition, higher power IPA's are in development (30-60W), along with IPA's incorporating higher levels of functionality.

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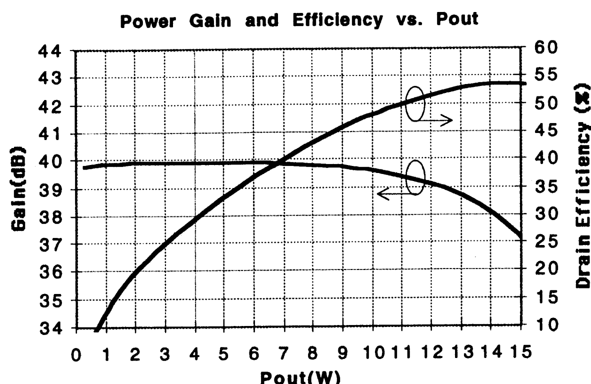

Fig. 7: Gain and PAE vs. output power for the 3-stage IPA operating at 26V, 950MHz. The 1dB compression point is at 12.6W with 52% PAE.

50V DEVICE DEVELOPMENT

Advantages of 50V operation include higher input and output impedance levels for a given output power (simplifying broadband amplifier design), along with higher peak power capability in a given package (advantageous for high peak-to-average modulation formats). Motorola has been developing 50V devices for the past several years, and will qualify a variety of products for the broadcast and cellular market during the year 2000. Development has focused on designing for excellent ruggedness (BV_{DSS}) of 120V minimum) while achieving the HCI performance target at these elevated voltages (the initial 50V platform is designed for an extrapolated Idq drift of <10% over 20 years).

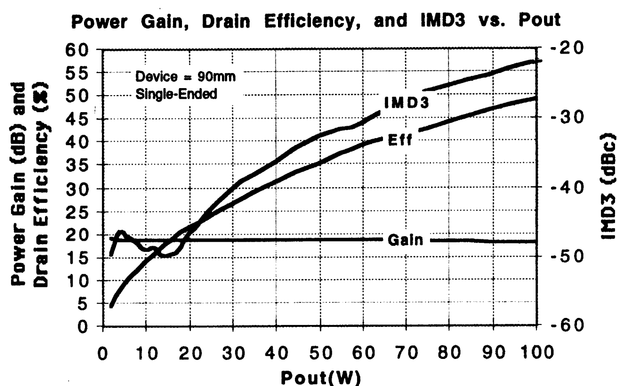

Fig. 8: Gain and drain efficiency vs. output power for a 90mm device operating at 50V, 945MHz. The output power at -30dBc is 60W PEP and 39% drain efficiency.

As an example of the performance, Fig. 8 plots the gain and IMD3 for a 90mm RF-LDMOS device operating at 50V and 945MHz, with a two-tone spacing of 100kHz. This device achieves 60W PEP at –30dBc with a gain of 18.6dB and a drain efficiency of 39%. This is nearly twice the power per mm of gate periphery of a 26V part. Note also the characteristic excellent backoff linearity.

CONCLUSIONS

RF-LDMOS is a leading device technology for high power, high efficiency linear power amplifiers. Essential details of the fabrication process have been described, along with a review of the key reliability considerations. The versatility of this technology have been highlighted in three applications: 1) a 28V, 220W P3dB push-pull device designed for WCDMA; 2) a 26V, 10W RF-LDMOS three-stage integrated power amplifier for the 900MHz GSM market offering 40dB gain and 52% PAE; and 3) a new 50V RF-LDMOS platform for the broadcast and cellular infrastructure markets. In addition to its excellent linearity and efficiency, the 220W transistor is, to our knowledge, the highest power Si-device ever reported for the 2GHz cellular market.

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