

Very High Efficiency and Low Cost Power Metamorphic HEMT MMIC Technology

P.C. Chao, K.C. Hwang, D.W. Tu, J.S.M. Liu, O. Tang and K. Nichols
Sanders, A Lockheed Martin Company
NHQ6-1551, 65 Spit Brook Rd., Nashua, NH 03061
pane.chao@lmco.com, (603)885-1057

Abstract

A successful development of a very high efficiency 0.1 μ m power Metamorphic HEMT (MHEMT) MMIC technology is reported. At 20GHz, an output power of 136mW was obtained with excellent power added efficiency of 60.2% and a record 17.1dB power gain. This device also produced an output power density of 0.51W/mm at $V_{ds}=3.5V$. At 60GHz, the MHEMT technology delivered 185mW (0.31W/mm) with a very high 41.2% power added efficiency and 6.9dB power gain in a single stage MMIC. These represent the state-of-the-art power MHEMT/MMIC results and are comparable to the best InP HEMT/MMIC performance. Since it uses a GaAs substrate, the MHEMT technology is scalable for 6" low-cost manufacturing.

Introduction

There has been considerable interest in developing low noise, high gain, high efficiency and high power transistor-based microwave amplifiers for both military and commercial applications. These high performance solid-state amplifiers provide circuit miniaturization, performance consistency and low power dissipation, all essential for successful system deployment. The highest performance devices/MMICs reported today use InP HEMT material and process technology. Performance achieved at Sanders includes 600GHz f_{max} and 1.2dB

noise figure at 94 GHz in discrete transistors. For MMICs, 219mW with 43% efficiency at 60GHz for single stage power amplifiers and less than 18mW power dissipation in a multi-stage X-band LNA, have been achieved. Although this performance is exceptional, the InP HEMT process is expensive to use and not readily scalable to manufacturing. This is because the InP substrates are difficult to process, more expensive and fragile than the GaAs substrates commonly used to manufacture MMICs. The InP substrates also are available only in 3 inch diameter, while low cost GaAs MMIC manufacturing is currently at 4 inch substrate diameter and is transitioning to 6 inch. In comparison, the processing technology for GaAs PHEMTs is more mature, higher yield and lower cost (presently 50% less). However, the power performance of PHEMTs is marginal and is much lower in efficiency and power gain (~10% lower efficiency and 2dB lower gain at 60GHz).

To address the needs for both high performance and low manufacturing cost, a novel new device, the metamorphic HEMT (MHEMT), has been developed during the past several years. This device employs the InAlAs/InGaAs active structure on a 3" GaAs substrate, and therefore can have the InP HEMT performance but with the GaAs wafer processing cost. Specifically, the MHEMT technology allows a production of very high performance devices/MMICs with only 10% of InP substrate cost and ~70% of InP HEMT wafer processing cost. The chip cost of

Table I Comparisons of power transistor technologies.

| Device Technology | Key Elements | Remarks |
|-------------------|--|--|
| GaAs PHEMT | <ul style="list-style-type: none"> • AlGaAs/InGaAs heterojunction • Channel In%: 15-30% • GaAs substrate | <ul style="list-style-type: none"> • Good reliability, mature technology • Low cost • Production ready |
| InP HEMT | <ul style="list-style-type: none"> • AlInAs/InGaAs heterojunction • Channel In%: 50-65% • InP substrate | <ul style="list-style-type: none"> • Increased PAE of amplifiers due to high device efficiency, high gain -PAE is critical parameter in most transmitters • Higher gain per stage results in reduced chip size (2/3) vs. GaAs PHEMT • Difficult to process, high cost • Not suitable for manufacturing • Reliability to be proven |
| MHEMT | <ul style="list-style-type: none"> • AlInAs/InGaAs/AlGaAsSb heterojunction • Channel In%: 30-65% • GaAs substrate | <ul style="list-style-type: none"> • GaAs-like processing • High gain and efficiency • Low cost, suitable for manufacturing • Flexibility of layer compositions provides higher breakdown and power than InP HEMTs • Reliability to be proven |

MHEMTs can be further reduced by 400%, if a larger size wafer (6") is used. (Note: 6" GaAs wafers are available, but only 3" is available for InP substrates.) Furthermore, the lattice constant shifting buffer growth technology in the MHEMT uniquely allows a wider range of Al and In compositions in the material structure, providing an excellent potential for even higher power performance (e.g., higher breakdown and output power) than that of the InP HEMT. Table I compares present microwave power transistor technologies.

Although the development history of the MHEMT technology is relatively short when compared to the InP HEMT, there have been numerous publications on the MHEMT technology with impressive small signal and low noise performance [1-6]. Excellent progress has also been made in the discrete power MHEMT device area. Specifically, a 1.5W output power at 950MHz was achieved with 63% P.A.E. with a 0.5 μ m, 35% In MHEMT [7]. Motorola has also reported the first enhancement mode 0.6 μ m power MHEMT (50% In) for single supply mobile communications: 59mW output power with

68% efficiency at 1V operation at 850MHz [8]. Most recently, a 0.15 μ m, 32% In double recess MHEMT has delivered an output power of 0.47W with 40% P.A.E. and 5.3dB gain at 35GHz [9].

In this work, we report an extremely high efficiency power MHEMT MMIC technology up to 60GHz. Our MHEMT has a patented AlGaAsSb strain relief buffer layer (~1 μ m thick) to eliminate lattice constant mismatch between the InP HEMT active layers and the GaAs substrate. Compared to other buffer technologies (e.g., As or P-based), the Sb-based buffer provides the best surface smoothness for MMIC processing. For very high efficiency performance, an In mole fraction as high as 65% in the device channel (in a strong contrast to 30-50% of others) was adopted in our layer structures.

Material Structure and Fabrication

A high-bandgap discontinuity InGaAs/InAlAs material structure - only realizable in metamorphic form - was used in this work to provide high power performance

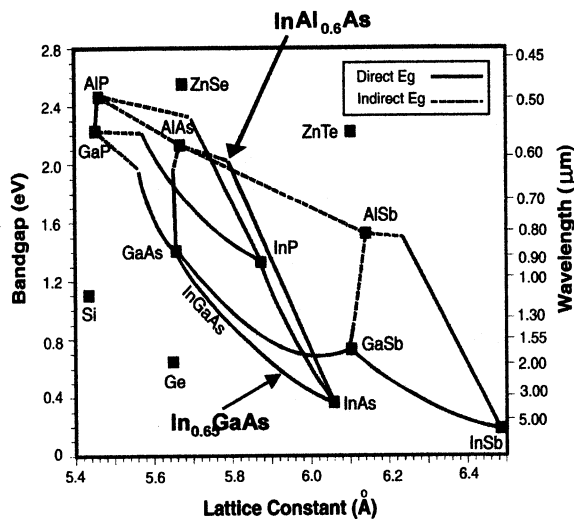


Fig. 1 Bandgap diagram of InAlAs/InGaAs system. The two arrows indicate the optimum layer compositions used in this work for largest bandgap discontinuity for optimum MMW high efficiency power performance. These compositions can only be achieved in the MHEMT structure.

at high frequencies. Fig. 1 illustrates our selection of the buffer/active layer compositions for best gain and efficiency at high frequencies.

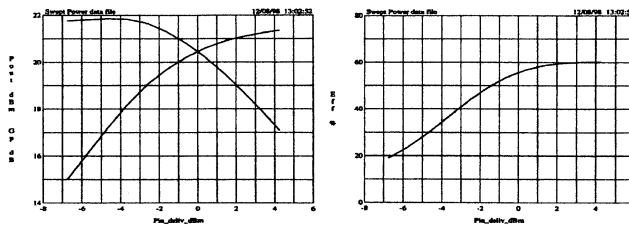
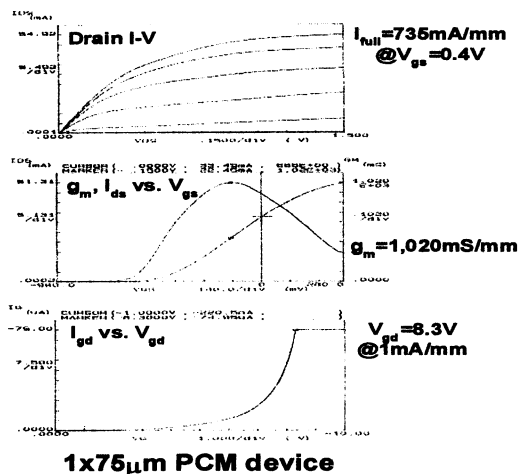
Mesa, AuGe-based ohmic, TaN resistor, Ti/Pt/Au T-gate, wet gate recess, Au-based liftoff airbridge, selective capacitor nitride deposition, slot via hole, and 2-mil thick substrate technology was used to fabricate MMICs. The gate recess was performed with a selective etchant to ensure uniformity across the wafer and higher yield of large periphery devices. The 0.1 μm T-gate was defined with E-beam direct write and the wafer was passivated with ECR nitride. Via holes for ground connection were dry etched with the RIE technique. Slot vias placed directly underneath each and everyone of the device source pads were as small as 15 μm in width. The small via hole size resulted in smaller gate finger pitch than what we can achieve with wet via hole etch. Large periphery cells can then be placed closer together to get improved phase matching when power combined. Slot via holes also provide direct source grounding for reduced source

inductance and improved thermal resistance - critical for V-band power applications. After DC/RF testing, wafers were finally diced through scribe and break.

MHEMT/MMIC Power Performance

Fig. 2 shows the DC and RF performance of a 0.1 μm double recess power MHEMT at 20GHz. The device has a typical transconductance of 1,000mS/mm with ~740mA/mm and >8V gate breakdown voltage. The device also has sharp pinchoff characteristics. At 20GHz, an output power of 136mW (0.46W/mm) was obtained with excellent PAE of 60.2% and a record 17.1dB power gain at 20GHz, (4x75mm device at $V_{ds}=3V$). This device also produced an output power density of 0.51W/mm at $V_{ds}=3.5V$. With a high In% in the device channel, a device transconductance as high as 1,800mS/mm has been demonstrated - ~2x higher of that of the typical InP power HEMT. Compared to our best double recess InP power HEMT, this power MHEMT has comparable output power density and efficiency but with a 2dB higher power gain at 20GHz.

In addition to the discrete MHEMT, we have fabricated a single-stage V-band power MHEMT MMIC. A single recess power MHEMT process technology was used for high gain in this case. As shown in Fig. 3, at 60GHz, the MHEMT technology delivered 185mW with a very high 41.2% power added efficiency and 6.9dB power gain in this MMIC. It should be noted the mask originally designed for InP HEMT process was used to produce this MHEMT MMIC. The above results represent the world's best-reported power MHEMT/MMIC performance. The higher device and MMIC performance (efficiency and gain) of this work is mainly due to the higher In% in the device channel, when compared to other power MHEMTs (e.g., 32-50% in [7-9].)



- Pout of 136mW (0.46W/mm) with PAE of 60.2% and 17.1dB power gain at 20GHz (4x75µm device at Vds=3V)
- Output power density: 0.51W/mm at Vds=3.5V

Fig. 2 K-band 0.1µm double-recess power MHEMT with excellent DC and power performance. The device has an exceptionally high power gain of 17.1dB at 20GHz. Maximum power added efficiency (P.A.E.) of 61% has also been achieved.

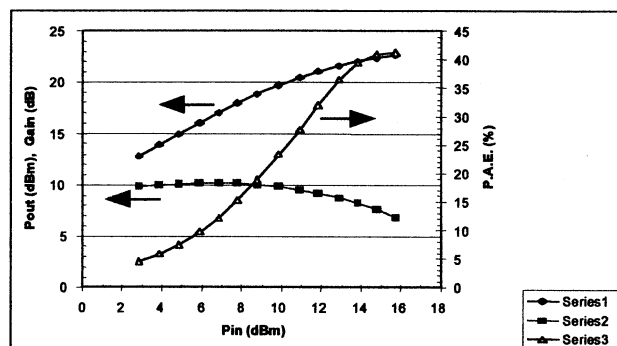
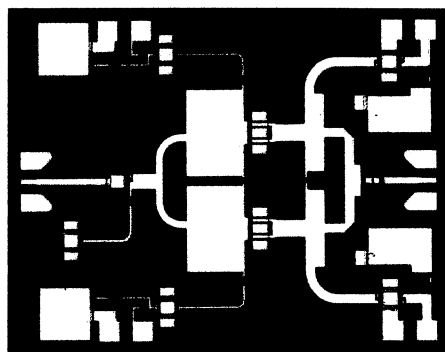


Fig. 3 First V-band 0.1µm power MHEMT MMIC with 185mW output power and >41% of P.A.E. at 60GHz. (Output stage: 8x75µm, biased at Vds=2.7V for maximum efficiency)

In summary, the potential of the power MHEMT technology for very high efficiency, high gain power applications at high frequencies has been demonstrated. The efficiency of our MHEMT device/MMIC is comparable to that of the best InP HEMT/MMIC and is ~10-15% higher than the GaAs PHEMT. With a GaAs substrate, the cost for the high performance MHEMT MMIC is expected to drop to \$1/mm² on the 6 inch manufacturing line, making applications such as phased array feasible for space based communications.

References

[1] M. Chertouk, et. al., IEEE Electron Dev. Lett., p. 273, June 1996.
 [2] Y. Cordier, et. al., 10th Int. Conf. on InP and Related Materials, p. 211, May 1998.

[3] H. Happy, et. al., IEEE Trans. Electron Devices, p. 2089, Oct. 1998.
 [4] S. Ballaert, et. al., IEEE Elect. Dev. Lett., p. 123, Mar. 1999.
 [5] K. Higuchi, et. al., IEEE Trans. Electron Devices, p. 1312, July 1999.
 [6] K. Hwang, et. al., IEEE Electron Dev. Lett., p. 551, Nov. 1999.
 [7] W. Contrata, et. al., IEEE Electron Dev. Lett., p. 369, July 1999.
 [8] K. Eisenbeiser, et. al., IEEE Electron Dev. Lett., p. 507, Oct. 1999.
 [9] C.S. Whelan, et. al., IEEE Electron Dev. Lett., p. 5, Jan. 2000.