Packaging Technologies for RFIC's: Increasing Integration

Albert C. Imhoff, Jr.
M/A-COM Semiconductor, a Tyco Electronics Company
100 Chelmsford Street, Lowell, MA 01851, USA
Phone:978-656-2657 , e-mail: imhoffa@tycoelectronics.com.

Abstract

In today's telecommunications market, competitive pressures are driving the electrical performance of RF integrated circuit (RFIC's) devices to new levels. At the same time, the demands placed on packaging of these RFIC's have caused more resources to be focused on solutions. The result has been that high frequency packaging is called upon to provide low cost, thermally efficient, miniaturized products for a wide range of wireless telecommunications applications.

The packaging of RFIC's covers a wide range of technologies, with a number showing promise for future developments. The end applications for these packaged devices range from fixed base systems to high portability, handheld uses. Both types require that aggressive performance and economic consideration be paid to packaging technique.

In looking ahead to the next generations of wireless products, a key determinant lies on the road to advanced packaging for RFIC's. System level integration and manufacturing technology for wireless products will likely remain primarily surface mount technology (SMT). With this constraint and cost considerations, increased level of integration will become the dominant issue.

Introduction

Designers of RF integrated circuits are faced with enormous pressures to develop circuits that provide optimum system performance. The choices of semiconductor technologies for RFIC applications make this development even more interesting; as competition between RF Si and GaAs technologies increases. In many instances multiple IC technologies exist to provide devices which fulfill a given requirement or system architecture. No less difficult in the development of RFIC's is the choice of packaging.

Packaging materials provide mechanical and environmental protection to the semiconductor devices they hold, but not without a price on circuit performance. As the frequency of circuit operation has increased the package and its electrical impact becomes more significant. The effect of this is that the package is an important element in the design of the RF device.

The growth of commercial and consumer wireless markets has caused the choices of packaging technologies to become more difficult in many ways. It is no longer practical to utilize the hybrid technology approach of glass and metal hermetic packages as a universal packaging medium. Packaging technologies are as diverse and applications driven as the semiconductor process technologies. The optimum match of device, package, and application requirements places RFIC devices among the most demanding components to produce.

Today's Applications Demand Higher Levels of Integration

In general, the considerations for RFIC packaging are like those for any digital device; thermal management, efficient utilization of package area for the motherboard, ready availability, acceptable environmental protection, component reliability, and overall economy are necessary items. Once these items are brought into focus by the application, the challenge of matching up device and package begins. Matching these effectively is a challenge and requires careful attention to the big picture.

The packaging technology options available today allow the designer to tackle applications with diverse requirements. The range of these requirements is reflected by the contrast between mobile applications and fixed base applications. Further demands of consumer applications versus industrial, commercial, or

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high reliability usage raise the degree of difficulty. Beyond providing the needed environmental and mechanical protection to the RFIC, the package must be readily compatible with test methods and technologies needed to assure product performance. While beyond the intended scope of this paper, RF test demands in very high consumer volumes are key elements to success.

Lastly, customers are decreasingly less willing to pay premiums for RF components and systems. In many cases, the traditional distinctions between a digital (commodity) semiconductor and a RF device have all but disappeared. This view is often reflected at the system level as well [1]

The Case for Increased Integration

A case history on the significant advantages in system packaging and cost is represented by thew evolution of a simple switch. This example illustrates the benefits of increased integration from the semiconductor through system level.

To illustrate the gains that can be made using advanced levels of integration, we will examine a SP4T GaAs based switch.

In an early generation of the system, military packaging techniques were employed to provide the high performance deemed necessary by the system design. The application for this device was a fixed station with ground based environmental requirements. The device performance requirements placed a high premium on isolation (better than 45 dBc). The SP4T was built using conventional military hybrid construction methods. The 0.625-inch square metal package employed glass seals and was hermetically sealed. The internal construction utilized thick film substrate with laser machined recesses for isolation performance. This technology represented the norm for military high performance packaging and was defined by the system specification. Manufacturing methods in the early production phases of the part were largely manual, with automation brought on-line in the later stages of the product life cycle. The part can be seen in Figure 1.

Once ready for the subsystem assembly, the SP4T was integrated onto a 14 layer, two sided assembly. The motherboard contained a number of printed passive elements to provide the need power handling capability.

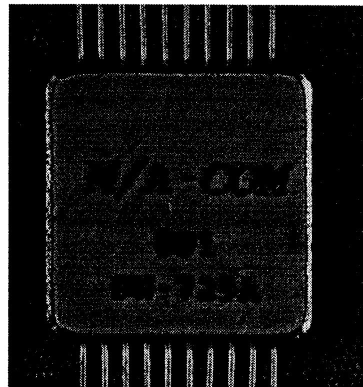

Fig. 1 SP4T Metal Flatpack

The PCB was very costly and the system cost was high. Twelve SP4T devices were for the system architecture. The motherboard was a typical RF subsystem. This assembly can be seen in Figure 2.

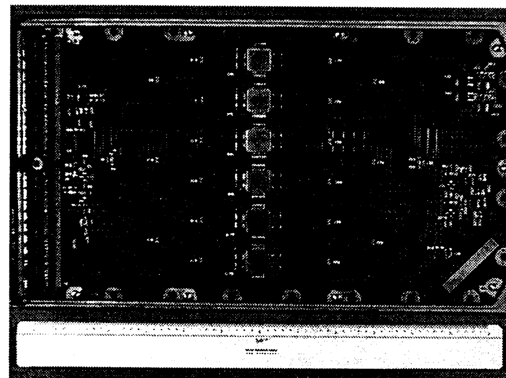

Fig. 2 Motherboard for SP4T Approach

Driven by cost considerations, the nex5t generation of switches combined the functionality of six devices into a single module. Using MCM-L technology significant gains in integration were achieved. The resulting 4x6-switch matrix module was made up of GaAs switches, silicon decoder/drivers, GaAs power dividers, and ceramic resistor networks. The module form factor was a 44-mm JEDEC PQFP. From the initial phases of this highly integrated module, automation formed a central part of the manufacturing process. The 4x6 switch is shown in Figure 3.

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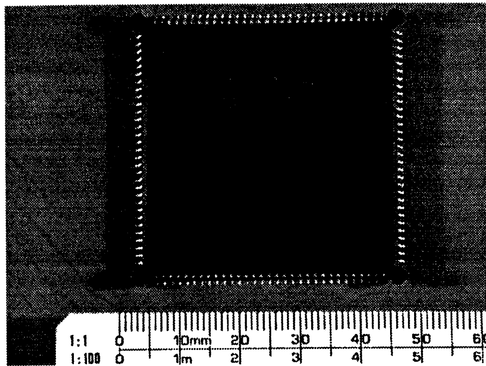

Fig. 3 44mm PQFP switch matrix

The module was screened in accordance to a specification tailored after conventional military requirements and subjected to an on-going reliability monitoring program throughout the production life cycle. The advantages of integrating the 6 metal flatpacks into a single MCM-L module did not stop at the device level. The motherboard was reduced to an 8 layer board; a substantive savings. The assembly was further reduced to a single sided assembly from a two-sided one. Figure 4 illustrates the cleaner, simplified result.

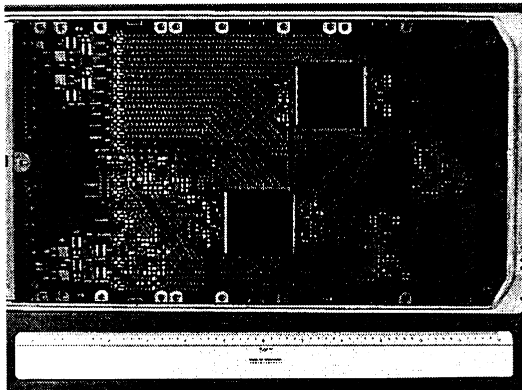

Fig. 4 Motherboard for PQFP module

The PQFP module approach provided significant improvements in integration at the semiconductor packaging and subsystem level over the metal flatpack technology. However, the PQFP was susceptible to lead damage in all phases of manufacturing and the leads presented complications in the substrate manufacturing process. Continuing cost pressures and increased performance demands led to further integration.

The next generation of the 4x6-switch module was realized using leadless packaging in the form of the ball grid array (BGA). The elimination of the leads produced benefits to virtually every phase of the manufacturing process. Further benefits in RF performance, particularly isolation were realized. The resulting component shown in Figure 5 is a 45 mm JEDEC PBGA. This device incorporated more highly integrated GaAs Asics to eliminate resistor networks and reduce the number of wirebonds. The resulting PBGA was subjected to a screening protocol of industry-standard JEDEC testing.

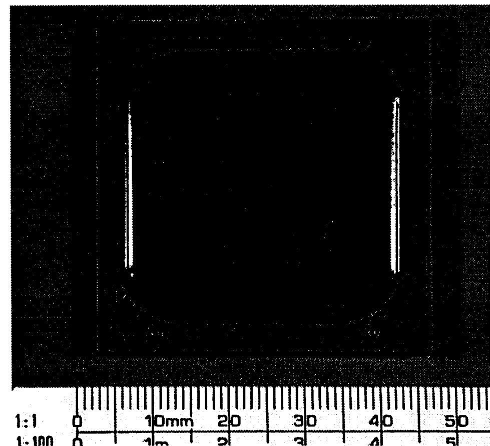

Fig. 5 45mm PBGA module

With the continuing demand for integration, leadless packaging has presents a number of advantages. The call for smaller RFIC packages often includes the incorporation of bias and matching circuits for improved performance and reductions in parts count.. The multichip module in the BGA format can provide RFIC packaging that has high levels of functional integration in a 50-ohm part. Modeling techniques of the package and effects are critical elements in the development of these products [3].

The resultant motherboard using the BGA is shown in Figure 6. It can be seen that there is a high degree of similarity to the PQFP version.

It is common for fixed base telecommunications systems to place 10 to 20 year life requirements on components. This requirement has slowed the adoption of advanced packaging techniques [5]. The standard BGA packages with 1 to 1.5 mm ball pitch have been shown to provide acceptable interconnect reliability. RFIC packages using

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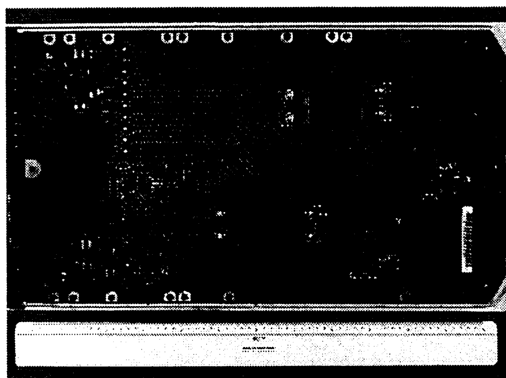

Fig. 6 Motherboard for PBGA

MCM methods can be used to provide system compaction while achieving high isolation and signal integrity. This has been shown at digital signal processing levels in high-speed processor applications [4].

Advanced Technology for More Integration

The benefits of sophisticated packaging techniques can be seen in the next generation of this product type. Figure 7 illustrates the effects of increased die level integration, reducing the integrated circuit count by 50%. The same functionality can now be provided in a 15-mm PBGA.

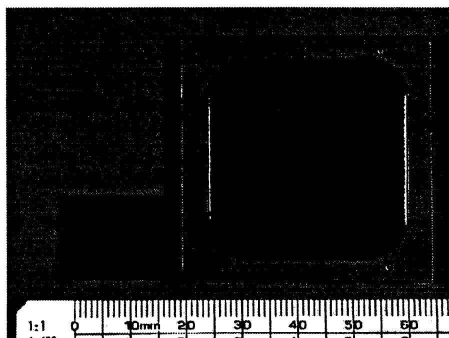

Fig. 7 Comaprison of 15-mm and 45-mm switch matrix parts

Further gains in the size of the subsystem can be seen in Figure 8 when the further integration is applied to the motherboard.

The use of advanced RF integration techniques has produced dramatic benefits in size reduction and manufacturing improvements. These accomplishments are worthwhile on their own. When combined with significant cost reductions, the matter of applying increased levels of integration makes advances in wireless product opportunities possible [6].

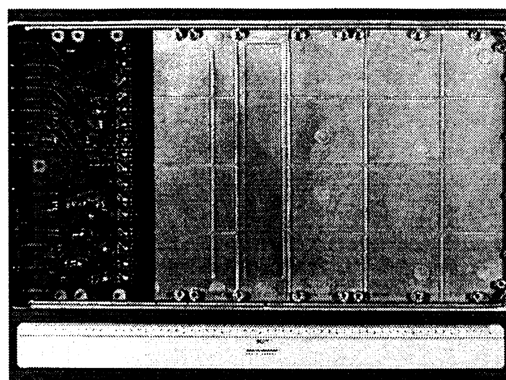

Fig. 8 Advanced switch matrix

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