Breaking the 1000 Wafers/Week Barrier Through Substrate Via Process

K.M. Adams, L.S. Klingbeil
Motorola Semiconductor Products Sector
Compound Semiconductor One; CS-1
2100 E. Elliot Road, Mail Drop EL-609 Tempe, AZ 85284
Phone-(480) 413-4825, FAX-(480) 413-5748, Email-Kevin.Adams@motorola.com

Abstract- The demand for compound semiconductor devices with low inductance through substrate via holes continues to increase as operation frequencies climb. However, the process used to fabricate through substrate via holes is not considered a high volume manufacturable process by silicon standards. The mechanical nature of the process and the severity of etching a via 25 to 100 times deeper than a traditional interconnect via presents challenges to maximizing volumes and keeping costs down.

Processing aside, manufacturing philosophies and monitoring tools can help increase volumes and lower costs considerably. These include the practice of Theory of Constraints or TOC, and the application of a standardized equipment performance metric, Overall Equipment Efficiency (OEE). Together with innovations from the equipment industry, high volume manufacturing of through substrate vias can be achieved.

I. Introduction

Breaking the 1000 wafers per week barrier for through substrate via processing may be the most challenging exercise for a GaAs fab. It simply takes hard work and analysis to transform a low volume, generally low tech process into one that can meet the demands of a growing cost competitive market. In two years time, the demand at CS-1 for this technology will increase twenty-two fold. In order to keep up with this pace, the process itself requires scrutiny from substrate mount through the final outgoing inspection. Capacity constraints and yield metrics identified by an assortment of manufacturing tools outline where creative new equipment, processes, and materials are required. The manufacturing tools used at CS-1 include the practice of the Theory of Constraints, and the application of Overall Equipment Efficiency. Together, the different disciplines of a factory come together allowing the breaking of one barrier and the preparation for the next.

II. Process Opportunities

A. Mounting Substrates

The thinning of III-V substrates to 15-100µm requires a hard mount to maintain rigidity through the backside process steps. The requirements for the mount are tied to the process used to fabricate the through substrate vias, the particular equipment, and the back metal scheme. Sapphire is a common mounting substrate because it is chemically resistant and transparent for backside alignment. It is so costly, especially at 150mm, that either an alternative material or a change in the process allowing a less expensive material to be used is essential to maintaining low processing costs. In the meantime, ensuring that all sapphires are the same thickness can eliminate unnecessary measurements and thus reduce stage cycle time significantly.

Wax alone or in combination with resist is commonly used for adhesive. To utilize existing equipment and process modules, such as a lead solder back metal scheme, a higher temperature adhesive is necessary. Such adhesive comes in rolls or large sheets and requires cutting at the mount stage. An area found to reduce material waste by 25% and reduce localized cycle time by 30% was to utilize pre-cut adhesive sheets made to exacting specifications. Moreover, automated mounting tools are becoming more available and may provide additional capacity and yield enhancements, although cost of ownership analysis has prevented testing of these tools at this facility to date.

Copyright 2000 GaAsMANTECH 2000 GaAsMANTECH Conference

B. Measurement Tools

Wafer thickness measurement tools are very simplistic during the research and development stages with limited capacity and a restricted budget. When volumes however exceed 500, 1000, or 1500 wafers a week, manufacturing analysis tools quickly identify the measurement steps as constraints. Wafer thickness repeatability is critical for process control in addition to device performance since passive element performance is impacted by change in its proximity to back metal ground plans. Therefore, a quick measurement system is required to ensure all wafers are within specifications.

A cassette to cassette measurement system by SigmaTech has been utilized to increase stage throughput by approximately 40%. The implementation of this step was by no means easy as custom equipment hardware and software changes were required before regular engineering intervention was eliminated. Much of the customization centered on our particular design of the mounting substrate and therefore may not be as big of an issue for other companies. This tool however can download information into a manufacturing tool called Datalog which calculates the amount of removal at both grind and polish etch.

C. Software Changes

Given the automation at the wafer thickness measurements and the automatic calculations on Datalog, another constraint is found; the grind tool. In the R&D mode all wafers were ground to the same amount followed by wet chemical thinning process using individual wafer targets. Each target could be entered into the SEZ tool since it was a single wafer processing tool. As production volume increases, a batch wet etch tool became necessary to maintain the production ramp. This means the individual wafer thickness targeting capability needs to move to the grinder. This requires new software to allow removal targets calculated by Datalog to be entered into the grinder by cassette location. The batch wet polish process could now be taken advantage of, resulting in over a 50% reduction in localized cycle time and a 97% increase in stage capacity. Moreover, a very significant cost saving is realized by not using the chemical hungry SEZ tool. It should be mentioned that if the mount process and sapphire uniformity are tightly controlled a batch grind process can also be taken advantage of.

Another tool set requiring software modifications is the cluster dry etch tools. Since multiple processes run on these tools with very different etch times, it is imperative that a cassette be changed when it completes processing. This is better than waiting for all the chambers to complete processing of each of their cassettes. Dedicating three chambers to one process across many tools was shown to impact throughput by limiting flexibility to process on-hand material. Throughput enhancements by utilizing the new software are estimated at around 15% however as of this writing, this opportunity has not been implemented.

D. Photo Processing

The masking of the substrate obviously depends upon the process method of creating the through substrate vias. Photo resist is a common method for applications using a dry etch. The resist thickness depends upon whether or not a hard mask is used and the selectivity of the dry etch process. Even with relatively excellent selectivity the resist thickness required to mask a 15-100µm deep via is substantial. A common method to remove resist stringers on the outer edge of the mounted substrate is chemical edge bead removal. A known drawback to this approach is the swelling of the resist along the wafer perimeter. And, although not significant for most 1µm resist applications, the swelling of a resist ten times as thick is very significant at the resist removal process.

The solution utilizes an optical ring incorporated into the 1x backside via mask so that the chemical edge bead removal process could be replaced with an Optical Edge Bead Removal process or OEBR. The photo process now requires one less process step saving time and chemicals, but the most significant improvement is to the dry resist removal process. A 64% reduction in cycle time and a 26.6% increase in tool capacity is realized though the OEBR implementation.

E. Demounting Substrates

The final and perhaps most stressful process, both to the wafer and the engineer, is the demount process. This is where the separation of the 15-100µm thick 150mm wafer with 15-100 thousand vias from the sapphire carrier takes place. Stories of push sticks and hot plates can be horrifying while hot solvent baths allowing wafers to float away make people think of Pringles potato chips. The desire was to have a batch demount process with absolutely no fractures and no chemical residues.

The resulting creation is a patented demount cell which fits into a slightly modified standard wafer cassette. Submerged horizontally in solvent, the wafer is gravitationally pulled from the carrier yet it is not permitted to bend or flex to the point of fracturing. Additionally, the entire cassette can be removed from the demount bath and placed into a standard dump rinse and spin rinse dryer without any harm to the wafer. Implementation of this process represents a 24-48x

Copyright 2000 GaAsMANTECH

2000 GaAsMANTECH Conference

improvement in capacity over the single wafer separation processes.

III. Manufacturing Tools

A. Theory of Constraints (TOC)

Beyond the technological development of a new process such as the through wafer via process, the enormous demand for this product made it vital to develop a process that would allow a seamless transfer into manufacturing. To accomplish this feat, manufacturing experience was drawn upon early in the development process to provide methodologies and philosophies to the development of the through wafer via process in CS-1. Because of the critical nature of the product, along with the low-tech and generally manual nature of the process, it was important to establish strong manufacturability from the beginning.

During the development stages of this process, the application of the Theory of Constraints (TOC) was utilized to uncover the potential roadblocks to high volume manufacturing. TOC, commonly known as Constraint Management or Bottleneck Management, is an improvement philosophy pioneered by Dr. Eliyahu M. Goldratt, who authored the management book called *The Goal*. The basic philosophy of TOC, and the basic difference to many other improvement philosophies, is the assumption that every system has at least one constraint, and that the performance of that system is limited by the output of the constraint. Given this assumption, TOC is often explained through the common analogy, "a chain is only as strong as the weakest link". What keeps a system from higher productivity is the weak link, therefore improvements made at the weak link are essential for overall system improvements. On the contrary, an improvement made to a process that is not the weak link is considered to be a "mirage".

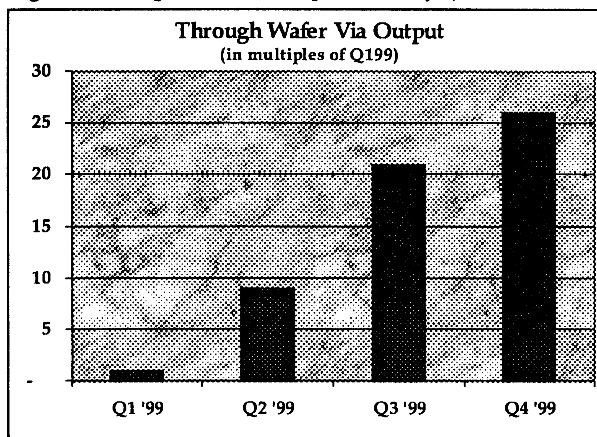
The TOC process of on-going improvement is based upon the Five Focusing Steps. These five steps include:

Step1 - IDENTIFY the system's constraint(s)
Step2 - EXPLOIT the system's constraint(s)
Step3 - SUBORDINATE everything else to the constraint(s)
Step4 - ELEVATE the system's constraint(s)
Step5 - Return to Step1, but beware of inertia

Using this process, organizations gain common sense solutions and methodologies to organize themselves to achieve the highest performance for the entire organization as oppose to individual departments.[1]

When applied to the through wafer via process, we were able to identify the process and/or equipment improvements necessary to improve the output of the entire process. Given our lack of infinite resources to improve every step of the process, the TOC methodology allowed us to focus only on the constraint of the process (or those identified as near-constraints), which in turn allowed us to achieve the productivity gains necessary to ramp production. Many of the process improvements that were attacked due to the results of our continued TOC focus may not have been a focal point of our efforts without our belief that these specific steps in the process were limiting the overall output of the process. As discussed earlier, many of the areas we focused upon were not technical in nature. By applying the principles of TOC, we quickly identified the need to improve the thickness measurement of the wafer/sapphire and to remove the requirement to grind and wet etch each wafer individually. With these improvements, as shown in Figure1, we were able to increase output of the through wafer via process by over 25X during the course of one year.

Figure 1. Through Wafer Via Output Plotted by Quarter: Used TOC



to identify throughput constraints.

B. Overall Equipment Efficiency (OEE)

After repeating the TOC Five Focusing Steps several times, the process eventually reached a steady-state, and one process was identified as the true constraint of the through wafer via process. All decisions regarding product movement were subordinated to the constraint, and the constraint tool becomes much more closely monitored to ensure the highest possible output.

One method employed to develop actions for improving throughput was the utilization of the Overall Equipment Efficiency (OEE) metric. The OEE metric is comprised of three equipment indicators; availability efficiency, performance efficiency, and quality efficiency. Availability efficiency is determined by equipment uptime. Any non-production time, such as unplanned / planned maintenance, routine equipment

Copyright 2000 GaAsMANTECH 2000 GaAsMANTECH Conference

qualifications, setups, etc., are subtracted from the overall equipment uptime. After the available hours are determined, performance efficiency is calculated by the ratio of how much product was processed during the available uptime to how much product theoretically could have been processed during the available uptime. Any throughput losses due to idle time or equipment not performing as efficiently as it should be, will be captured in the performance efficiency category. The third category of the OEE metric is quality efficiency. Yield losses due to scrap and rate of rework combine to determine the quality efficiency. The Overall Equipment Efficiency is then calculated by multiplying the three categories;

OEE = Avail Eff * Perf Eff * Quality Eff

Daily monitoring of the OEE will reveal where productivity losses occur, and where the largest opportunities of improvement lie. Applied with the basic philosophies from TOC developed from the foretelling line from *The Goal*, ". . . an hour lost at a bottleneck is an hour lost for the entire system", the areas of improvement identified by OEE will ultimately increase the throughput of the entire process. [2,3]

Our tracking of OEE at our system constraint identified two major areas of improvement, availability efficiency and performance efficiency. The availability efficiency data gathered by our OEE tracking was shared with our equipment vendors, and with a joint effort, availability efficiency climbed over time. Our poor performance efficiency was primarily driven by excess amounts of equipment idle time. Because of the manual nature of the entire process, the manufacturing team responsible for the through wafer via process would not always ensure the constraint tool was continuously running. Once we identified the tool as the true constraint and started to monitor the OEE performance, we quickly shifted the paradigm and improved the performance efficiency. Figure2 below is an example of an OEE chart that was used to identify improvement opportunities at our constraints.

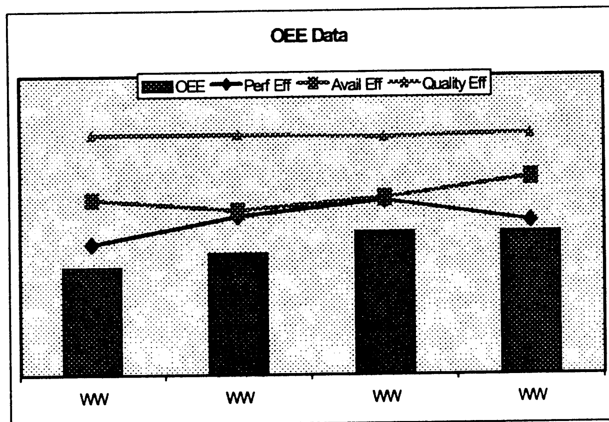


Figure 2. OEE Metrics Plotted by Work Week: Used to drive OEE Team Goals Necessary to Meet Production Output.

IV. Conclusions

A summary has been made of observations found during the transition time from R&D to very high volume manufacturing with cost considerations. The team of people working on the through substrate via process have reduced theoretical cycle time by 29% and increased capacity by over 40% - no equipment added calculation. Although many III-V fabrication facilities utilize the through substrate via process, the subtle differences may indicate an alternative direction to improve manufacturability. Hence manufacturing tools used at more mature fabrication facilities needs to be utilized in order to identify opportunities and meet the aggressive III-V market demand.

Acknowledgments

We would like to thank Chris Rummel, Cole Eberson, Susan Valocchi, Terry Daly, Brent Bogue, and others who participated on the substrate via program for their technical and manufacturing contributions.

[1] Avraham Y. Goldratt Institute, http://www.goldratt.com

[2] The Goal: A Process of Ongoing Improvement, E.M. Goldratt, J. Cox, North River Press, NY, 1986

[3] Manufacturing Methods Council Meeting, International Sematech, June 1999

Copyright 2000 GaAsMANTECH

2000 GaAsMANTECH Conference