New On-Wafer Digital Laser Trimming Technique for Current Adjustment of GaAs FET

Yukio Iwasaki, Hidetoshi Furukawa, Tsuyoshi Tanaka and Daisuke Ueda

Semiconductor Device Research Center, Matsushita Electronics Corporation
3-1-1 Yagumo-Nakamachi, Moriguchi, Osaka, 570-8501, JAPAN
Phone: +81-6-6906-4923, Fax: +81-6-6907-2640
E-mail: iwasaki@oerl.src.mei.co.jp

Abstract

New on-wafer digital laser trimming technique has been developed for accurate and high-speed DC bias current adjustment of GaAs FET. The trimmable resistor is included in FET chip and small enough to be arranged between bonding pad area. The adjustment of bias-current is made by once exposure of pulsed YAG laser. Digital trimming can be performed during the wafer probe-testing, where the appropriate trimming pattern is selected by comparison of measurement and pre-set value. This technique has high throughput and no area penalty.

INTRODUCTION

Digital communication systems are gaining in popularity since they can support more subscribers by using TDMA and CDMA than analog one. In the handsets for these systems, GaAs FETs are widely used as the power amplifier. In view of designing GaAs power FETs, high efficiency is the most important feature in order to realize long battery life. For this purpose, heterojunction FETs (HFETs) have been developed because of theirs high performance[1-4].

There has been much effort to control the drain current/threshold voltage, such as using selective dry or wet etching techniques. For HFETs, it is crucial to control the threshold voltage precisely due to the inherent deviation of thickness and doping concentration. The improvement of etching process is not sufficient to decrease the deviation of the drain current/threshold voltage. For this reason, analog laser trimming of off-chip bias resistors has been widely used in conventional power amplifier (PA) for adjusting the quiescent-current. However, such adjusting technique has poor throughput and need a large trimmable resistance area.

In this work, we have developed on-wafer laser trimming in a digital manner with high throughput and no area penalty. The on-chip bias resistors which are made of WSiN thin film can be laid out between bonding pads. It contributes to downsizing complete PA without increasing the chip size. The proper combination of bias resistors can be selected by the controller units based on a pre-set parameter. The combination is realized on each FET chip by once exposure of pulsed YAG laser through the selected shutter pattern. This results in dramatically enhanced uniformity of the bias-current with high throughput.

ON-WAFER DIGITAL LASER TRIMMING SYSTEM

The trimming system consists of optical system, automatic prober, current/voltage source and computer for controlling all system. The flow chart and schematic figure of the system is shown in Fig. 1.

The light source is YAG pulse laser (λ=1064nm). The light is not absorbed by GaAs substrate but absorbed by only the trimmable resistor. There is no damage to GaAs substrate. The photograph of optical system is shown in Fig. 2. There is the mask with some apertures between light source and the wafer. The light is expanded by the optical lens to cover the all apertures with good uniformity. The expanded light through the apertures is focused on the trimming area of selected resistor pattern. The shutters are moved by piezo devices.

The flow of the bias-current adjustment is as follows. The current-voltage characteristics are measured by the initial probe-testing. Proper resistance, which gives certain drain current, is computed according to the characteristics. The controller selects 5-bit digital shutter pattern and moves the shutters above the apertures. The YAG laser trims selected resistors on the chip. As a result, proper resistance is realized on the chip by rest of resistors. It is noted that the adjustment of bias-current is made by once pulsed laser exposure. Finally, drain current is confirmed and automatic probing stage moves to next chip. The advantage of the new trimming technique is short trimming time compared to conventional one. The conventional technique costs 5-7 sec to trim the resistors. On the other hand, the new technique with digital manner costs about 2 sec to adjust the drain current. Moreover, digital trimming can be performed during the wafer probe-testing. This technique has high throughput.

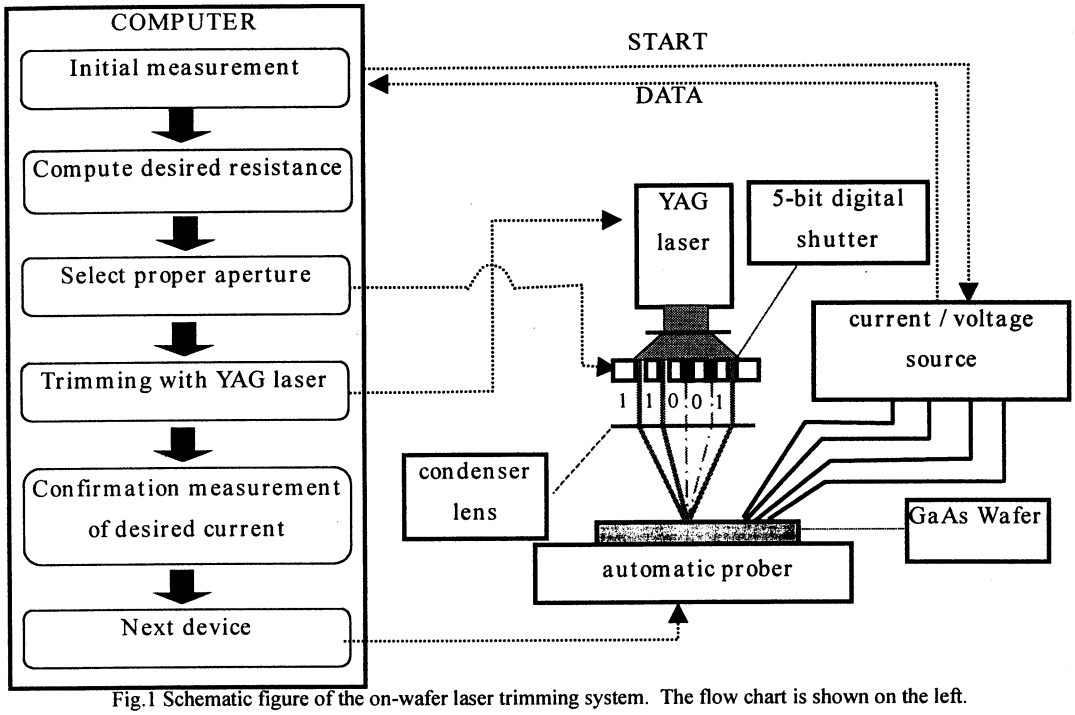

Fig.1 Schematic figure of the on-wafer laser trimming system. The flow chart is shown on the left.

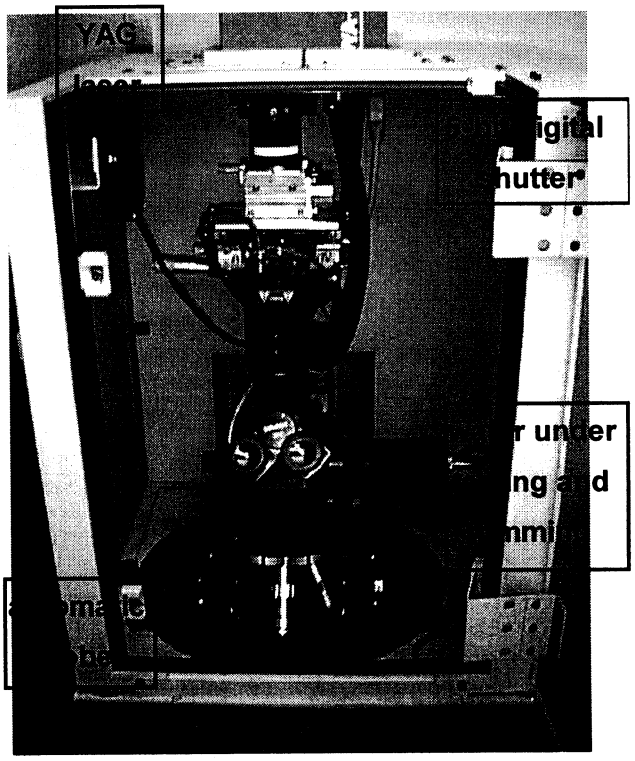

Fig. 2 Photograph of the on-wafer laser trimming system.

TRIMMABLE RESISTOR

The PA requires two off-chip bias resistors in conventional trimming technique. On the other hand, the bias resistors are included in FET chip in the new technique. Trimmable bias resistor is small enough to be arranged between bonding pad area. This technique has no area penalty.

The circuit diagram of the chip before the laser trimming is shown in Fig. 3. The biasing circuit consists of constant resistors R0, R6 and trimming resistors R1-R5 with different resistance. All resistors are made of WSiN thin film with

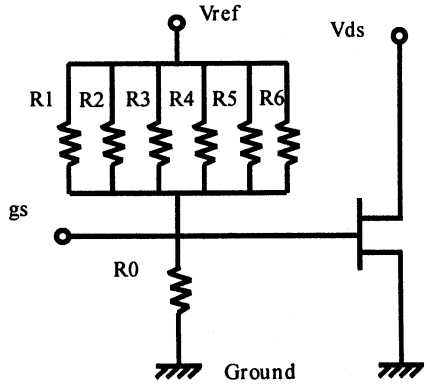

Fig. 3: A power FET with trimmable bias circuit used for on-wafer laser trimming

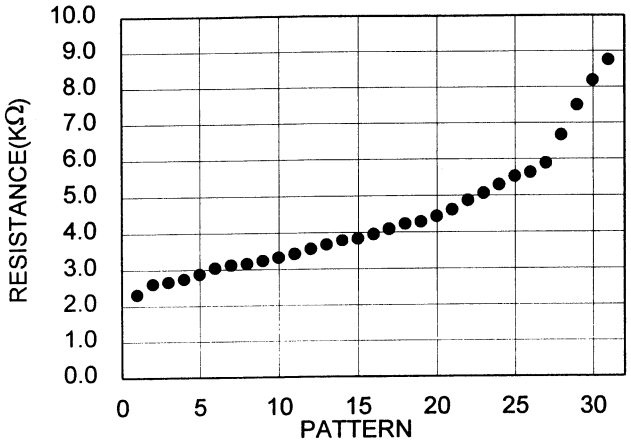

Fig.4 Resistance vs. the pattern of trimming resistor-network.

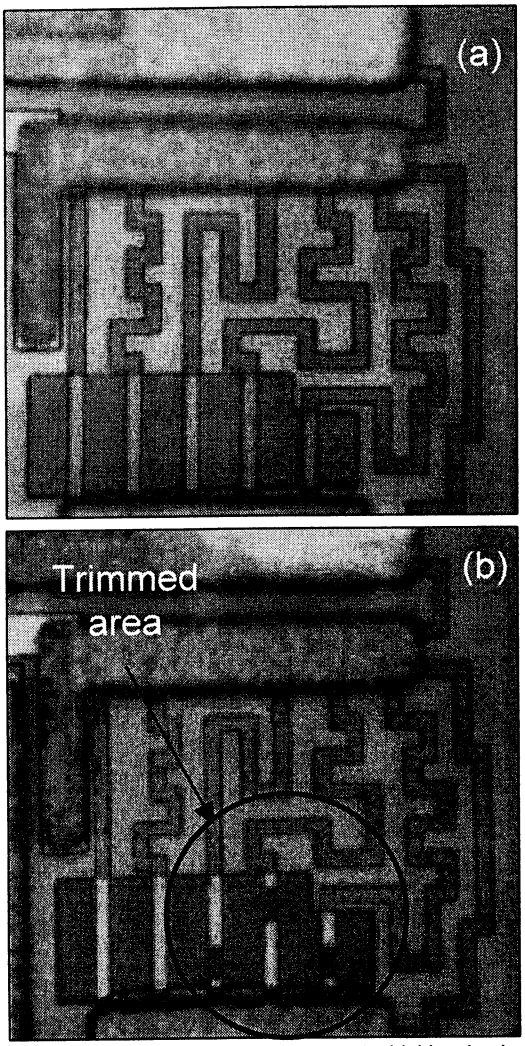

Fig 5 Microphotographs of power FET with bias circuit before (a) and after trimming (b).

the thickness of 100 nm.

As each resistor has two states which is "trimmed" or "untrimmed", the 5-bit parallel trimming resistor-network can have 32 (2^5) patterns resistance. Each trimming resistor is predetermined in order to change the parallel resistance from 2K to 6K ohm smoothly according to the shutter patterns.

Figure 4 shows the change of resistance in the parallel trimming resistor-network correspond to the patterns of trimming resistors. R_0 resistance was 3.3KΩ. R_1,R_2 R_6 resistances were 9, 12, 15, 18, 21, 15 KΩ, respectively. Between pattern 1 and 27, the whole resistance of parallel-network changes very smoothly.

Figure 5 is the microphotograph of the biasing circuit before and after the trimming. As shown in the figure, the resistors are selectively trimmed by the laser. Thin film resistors have same width and different length. It should be noted that this configuration can cancel the temperature dependence of the biasing circuits. Because the fix resistor R_0 and the trimmable resistor have same temperature dependence.

SAMPLE PREPERATION

The GaAs power FET with the parallel trimming resistor-network was fabricated by following process flow. Device processing began with standard mesa formation to active region. SiO_2 deposition was performed by chemical vapor deposition. The SiO_2 layer is 400 nm thick. Conventional Au/AuGeNi metallurgy was used for source and drain electrodes which were defined by lift off using the SiO_2 as the spacer. The electrodes were subsequently alloyed with GaAs. The gate recess was formed by wet etching and the Al/Ti gate electrode was formed by lift off. SiN film was deposited as spacer by plasma assisted chemical vapor deposition. WSiN thin film was deposited on SiN film by DC sputtering. The sheet resistance of WSiN thin film is 450 Ω/ . The resistor patterns were made by photolithography technique. The thin film was etching by reactive ion etching process using photoresist as etching mask. After interconnecting of gate fingers by Au electro-plating, the FET was passivated using 100 nm-thick SiO_2 and 400 nm-thick SiN. Finally, passivation films were removed over trimming area by dry and wet etching process.

ADJUSTMENT RESULTS

Figure 6 shows distribution of the drain current before the laser trimming under biasing Vds=3.5V and Vref=–2.25V. There is much deviation under same basing condition in each FET. The initial standard deviation of the drain current is 298 mA. This deviation of drain current based on no uniformity of threshold voltage.

Figure 7 shows distribution of the drain current after the laser trimming. The target of drain current was 300±50mA. This is standard condition in conventional laser trimming

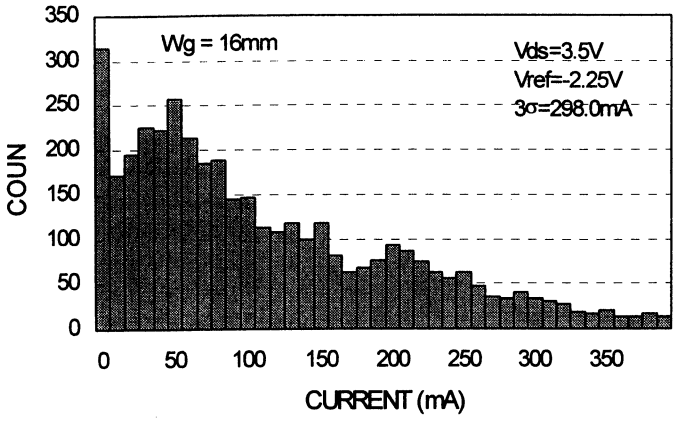

Fig.6 Distribution of drain current before trimming

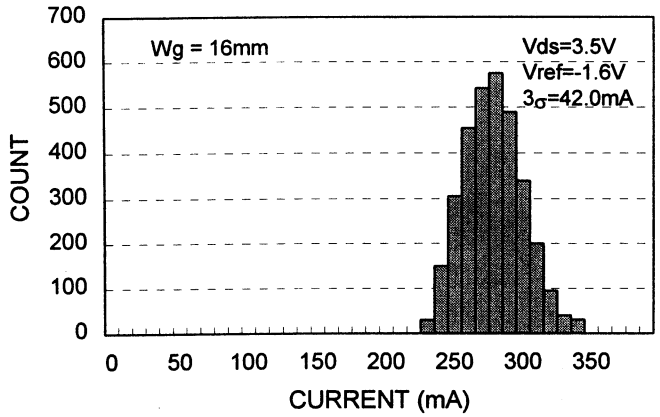

Fig.7 Distribution of drain current after trimming

after trimming, the drain current distributes among the adjustment range. The standard deviation of the drain current is reduced to 42 mA for the reference voltage of −1.6V. This current deviation is sufficient for precise power control of RF amplifiers.

CONCLUSIONS

We have developed on-wafer laser trimming with digital manner. The bias resistors are included in FET chip. Trimmable bias resistor is small enough to be arranged between bonding pad area. The resistance of parallel-network changes very smoothly. Because trimming resistors have difference resistance each other and trimmable parallel resistor has constant resistor. The YAG laser is absorbed by only the WSiN trimmable resistor. There is no damage to GaAs substrate. After laser trimming, the initial standard deviation of the drain current, 298mA, is reduced to 42mA for reference voltage of −1.6V. This on-wafer digital laser trimming technique has great potential for a variety of GaAs FETs and MMICs with high throughput and no increase of the chip size.

REFERENCES

[1] N. Iwata, K. Inosako and M.Kuzuhara, IEEE MTT-S Digest 1445 (1993)
[2] P. Smith, L. Lester, P. Chao, B. Lee, R. Smith, J. Ballingall and K. Duh IEDM Tech. Dig., 133 (1987)
[3] N. Iwata, K. Yamaguchi and M. Kuzuhara, Solid-State Electronics 41, 1587 (1997)
[4] T. Tanaka, H. Furukawa, H. Nagata and D. Ueda, Solid-State Electronics 43, 1405 (1999)