Assessing Circuit Hermeticity By Electrolysis

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ABSTRACT:

This work describes a corrective action project to improve circuit hermeticity. The objective was to provide quick feedback on experiments to improve performance in biased humidity environments. The ultimate goal was to improve hermeticity to the point that enhanced circuits could withstand an accelerated biased humidity qualification test in plastic encapsulated packages. Hermeticity was evaluated quickly by using current flow (electrolysis) in water applied directly to the surface of the devices. Weaknesses in device construction were discovered, and effective solutions were evaluated, by using the electrolysis technique.

INTRODUCTION:

In the semiconductor industry, standard reliability qualification testing includes one or more humidity evaluations. These evaluations subject an appropriate sample of devices to a humid environment (64% to 100% relative humidity) in combination with one or more of the following: elevated temperature, bias, and/or pressure. This project began with the unanticipated failure of devices in a test hereafter named "HVZPM" for **High Voltage, Zero Power, and Moisture** test. This result was unexpected since many previous humidity tests (including those more severe than HVZPM) have passed without incident. Two unique aspects converged to bring about the initial failure.

Process. The devices in this study are fabricated using a newer generation foundry airbridge process, which utilizes thick plated gold metallization. The airbridges are 4 um thick, and the bottom interconnect layer (metal one) is 2 um thick. Nitride interlayer dielectrics and passivation are used to seal the structures at various steps. This process was originally qualified for production by wafer-level tests conducted on PCMs (Process Control Modules). No difficulties were encountered during the qualification testing, which included a standard 96-hour unbiased 100% humidity, 121°C, 15 PSI, autoclave test (on whole wafers).

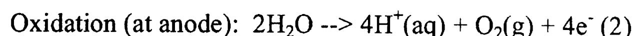
Bias. The bias selected for the HVZPM testing is historically unique. The test is conducted with 4.7 Volts across the FET channels and the gate pulled off hard beyond –4 Volts. The bias was intentionally selected by the customer to include high voltage (>8 Volts) and zero power dissipation (<<1mW). While this bias meets both the letter and spirit of the JEDEC 85°C/85% relative humidity specification (JESD22-A101), it does represent a new (and until now, un-reported) regime of humidity testing. Note that this is particularly applicable for RF power amplifier testing.

METHODOLOGY:

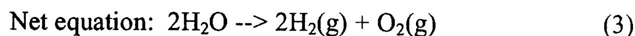
This project began with a challenge to develop a humidity performance improvement in the shortest possible time. The results had to include an extended evaluation phase (HVZPM testing) for final acceptance. Several accelerated evaluation techniques were attempted. Eventually, the electrolysis (bubble) testing was found to be applicable throughout.

The use of electrolysis to evaluate hermeticity is unpublished, but the technique has been used for many years in the semiconductor industry. Electrolysis is an electrochemical process by which electrical energy is used to promote chemical reactions at electrodes. In simpler terms, electrolysis is the decomposition of a compound (water) by passing an electric current through it. If pure water and chemically inert electrodes are utilized, the decomposition results in hydrogen and oxygen gas. The reduction and oxidation reactions are:

Reduction (at cathode): $2(2H^+(aq) + 2e^- \rightarrow H_2(g))$ (1)



Oxidation (at anode): $2H_2O \rightarrow 4H^+(aq) + O_2(g) + 4e^-$ (2)



Net equation: $2H_2O \rightarrow 2H_2(g) + O_2(g)$ (3)

Additional reduction and oxidation reactions can occur using special electrolytes and/or electrodes that are reactive. For example, this type of reaction in a gold-cyanide or gold-sulfide bath is how interconnect is typically electroplated for thick gold metallizations.

According to Faraday's law, the decomposition voltage is:

$$\frac{285{,}800\ \text{Volt - coulombs}}{2 \times 96{,}540\ \text{coulombs}} = 1.480\ \text{Volts} \quad (4)$$

In this study, vigorous reactions were microscopically observable at around 5 Volts. Using the particular circuit of interest and 10 Volts reverse bias, water currents between 50 uA and 600 uA were observed. Experimentation has shown that this electrolysis reaction is very invasive in circuitry. Compared to other chemical reactions, such as acid decapsulation or gold metal etching, the electrolysis reaction is best at finding breaches in nitride passivation layers. For the purposes of this study, any passivation that prevents the occurrence of electrolysis shall be considered hermetic. In other words, no electrolysis bubbles means the seal is hermetic, at least for the 15-minute duration of the electrolysis testing.

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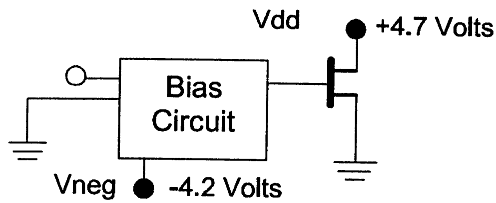

Figure 1. HVZPM Circuit Bias.

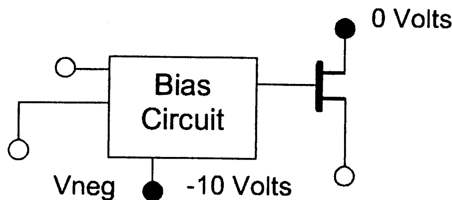

Figure 2. Typical Electrolysis Circuit Bias.

The electrolysis testing was performed on PCMs and circuits. PCM data was easy to interpret because of the separation of process layers in the various test structures. However, the circuit became the vehicle of choice because it is what fails in HVZPM testing. Eventually, three structure segments were observable and quantifiable as sources for the electrolysis bubbles: 1) LAB = Landed AirBridge, 2) FET = airbridge structures over interdigitated FETs, and 3) MET1 = Metal 1 (one) interconnects. For each wafer, three die sites were selected: A) near the edge (~1cm), B) mid-radial (~3cm), and C) near the center (~4.5cm). Each of the three die were probed, a drop of deionized water was applied, and then biased per Figure 2. The types of bubble locations were counted at each site after the elapsed time of 1 minute, 5 minutes, 10 minutes, and 15 minutes.

FAILURE MECHANISM

The HVZPM test failure mode is increasing gate current. Operationally, this causes an unstable bias situation which can overstress the large FETs utilized in the design. The overstress will typically mask or destroy the failure initiation site(s). Two separate HVZPM failures have been analyzed precisely to the failing element. In both of these analyses, the failure site was determined to be in the larger interdigitated FET structures. Numerous analyses of electrolysis test sites have determined that the common moisture path into the circuitry is through a crack at the base of the landed top metal. Photos 1 and 2 are two electron micrographs (prepared from Focused Ion Beam cross-sections) of those cracks before and after bubble testing. These micrographs show the primary cracks and evidence of the electrolysis by-products moving through the cracks.

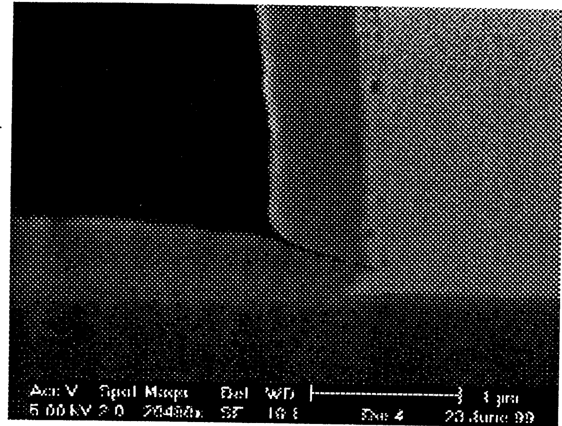

Photo 1. Typical Bubble Initiation Site.

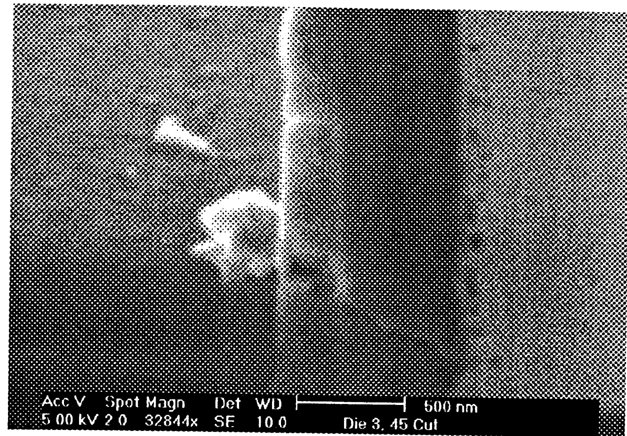

Photo 2. Typical Bubble Initiation Site With Debris.

RESULTS:

Initial brainstorming produced several experiments that were tested using several techniques. The potential cause list and test methodologies were modified upon initial results. For example, once the initial samples were tested, focus moved to upper layers of the process and thermal stress was found to have no effect. Following are short summaries of the results in chronological order:

Process Isolation. These experiments were intended to address three main questions: 1) how does hermeticity change at various steps in the process? 2) what is the best accelerated method of assessing hermeticity (gold etch or bubble testing)? and 3) how does high temperature influence the hermeticity? Sample wafers were pulled from 5 different runs as they progressed through the fabrication process. Separate samples were subjected to KII_2 (Potassium Iodine Iodate) gold etch and bubble testing. The results showed that at early steps in the process, the wafers are not hermetic (susceptible to both gold etchant and electrolysis bubbling).

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Testing of wafers later in the process showed that the wafers were hermetic, i.e. no KI_2 gold etch sites and no bubbling. However, after final passivation (before bond pads are etched) the wafers were no longer hermetic. This meant hermeticity was lost at airbridge metal formation.

Testing before and after a high temperature exposure resulted in no change in hermeticity. Eventually, side by side testing using KI_2 gold etch and the bubble method found that bubble testing was more sensitive, i.e. more sites would bubble than would be attacked by a gold etch. The following results are based on hermeticity evaluation by bubble testing.

Radial Effect on Hermeticity. Bubble tests on multiple lots have shown that hermeticity is compromised more at the edge of wafers than in the center. The majority of wafers were found to have more bubbling sites near the edges than in the center. Figure 3 shows the radial effect for a group of five random wafers. Figure 3 also shows the relative occurrence of bubbling (with time) from the three structure topologies that are possible breach locations on wafers in this study.

Bond Pad Photoresist. Bubble tests on multiple lots have shown that hermeticity is compromised by the bond pad etch process. Experiments on two lots have shown that a thicker photoresist reduces the damage at the bond pad etch step. (See Figure 4.) This was one of the significant results of this project. It was determined that the original photoresist was not adequate, and hermeticity was degraded during the bond pad etch step. The bond pads are overetched considerably in this particular process because all the nitride layers are removed in the scribe streets during the bond pad etch step.

Airbridge Process. Bubble and gold etch experiments have shown that hermeticity is significantly compromised by normal processing after the airbridge post photo step and before passivation nitride is added. More than half the lots inspected had bubble sites from metal one after airbridge, even though they had exhibited perfect bubble performance following metal one processing and passivation.

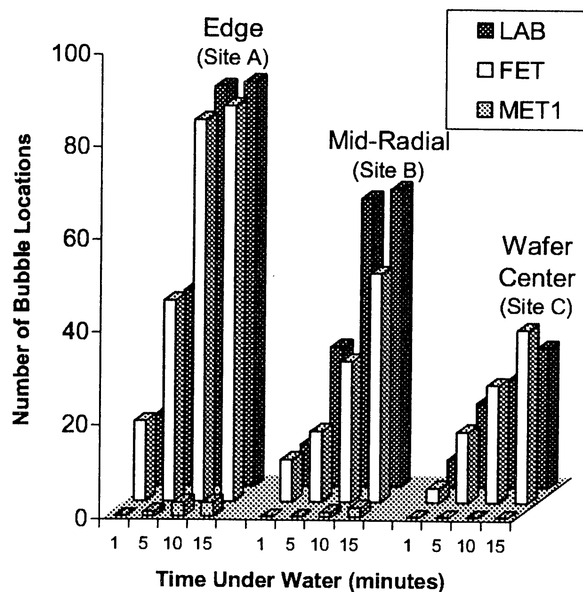

Figure 3. Composite of Bubbling Sites by Location on Wafer (Cumulative for 5 Wafers Before Optimization).

Packaged Part Testing. Several packaged parts were examined after decapsulation using a hot sulfuric/nitric acid etch. These decapsulated samples were found to have a large number of bubble sites, regardless of prior history. For example, devices exposed to HVZPM behaved similarly to good virgin devices. Likewise, samples passing HVZPM behaved similarly to devices which had failed during HVZPM exposure. All samples were non-hermetic. These results indicate either: 1) The decapsulation process causes loss of hermeticity, or 2) Assembly processing after wafer completion causes loss of hermeticity, or both.

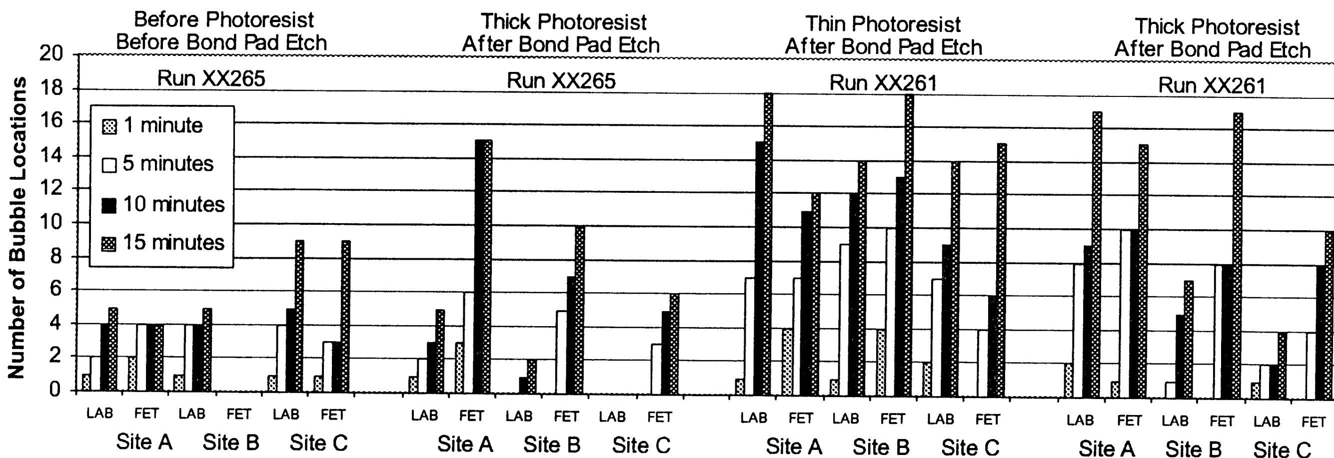

Figure 4. Loss of Hermeticity Through Bond Pad Etch Process, Comparing Use of Thick and Thin Photoresist.

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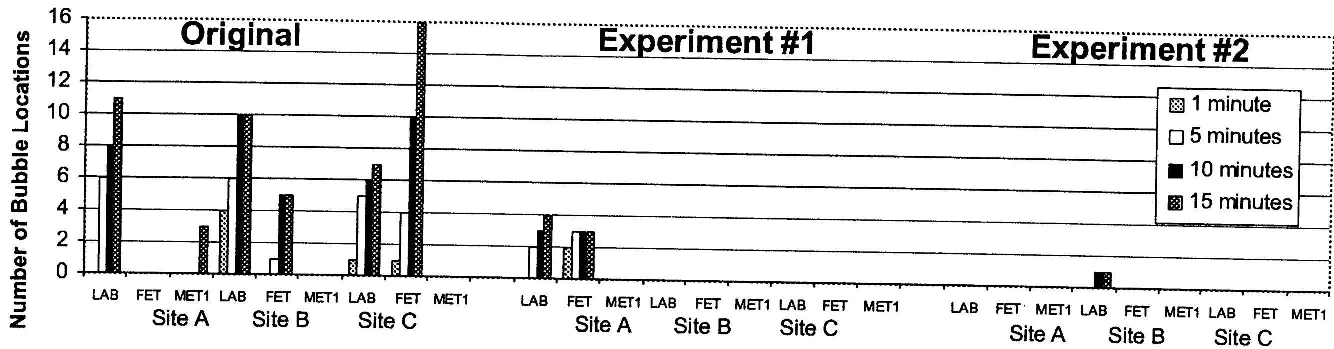

Figure 5. Number of Bubble Sites per Wafer Vs. Improvement Experiment.

Improvement Experiment. Bubble tests on three separate lots have shown that after a process improvement, the number of bubble sites is significantly reduced. KII_2 gold etch tests were also performed on wafers with different experiments. The KII_2 test showed some level of improvement with these experiments, but there were very few gold etch sites to compare.

At this point, it was once again determined that bubble testing was a superior (harsher) test for hermeticity by finding more openings in the passivation than a gold etch.

The dramatic decreases of bubble sites after Experiment #1 and Experiment #2 are the major breakthroughs of this study. The improvement of both experiments is strongly evident in Figure 5. This experiment was repeated on two additional lots with identical results and the process was updated. Experiment #2 has produced consistently hermetic wafers with one or fewer bubble sites on every lot.

Follow-up. Packaged part aging under HVZPM conditions has been completed on multiple lots incorporating the Experiment #2 improvement. These lots have completed testing successfully.

DISCUSSION:

Using electrolysis testing as an evaluation method for semiconductor hermeticity, this investigation has found three specific sources of hermeticity loss during processing. 1) Wafers are non-hermetic during early processing steps, but are eventually sealed. 2) Hermeticity is lost between airbridge post etch and final passivation steps. 3) Bond pad etch did cause hermeticity loss before the photoresist was thickened.

The process enhancements of thicker bond pad photoresist, and use of the process implemented in Experiment #2, results in hermetic die all the way through the fabrication and assembly process – a significant improvement. These hermetic products have subsequently survived 500 hour HVZPM testing in final packaged form.

CONCLUSIONS:

This work describes how electrolysis testing was utilized to evaluate circuit hermeticity and gauge the effectiveness of experiments conducted to improve humidity performance. Ultimately, the "bubble test" was found to be a good evaluation tool, in that wafers passing the electrolysis test could also pass long term HVZPM test in packaged form. Each of the following conclusions were determined from the project described here:

1. Moisture paths do exist in early processing, but wafers are hermetic after inter-layer-dielectric and metal one nitride layers.
2. Before optimization, moisture paths to airbridge metal existed when airbridge metal was applied and passivated.
3. Bubble testing is more aggressive in delineating hermeticity breach locations than gold etching (KII_2).
4. Moisture paths existed to metal one before thicker bond pad photoresist was used. The original bond pad photoresist was not thick enough. The bond pad etch would cause more pathways for electrolysis – some reaching to metal one. A change to thicker bond pad photoresist improves hermeticity and eliminates pathways to metal one.
5. Application of either Experiment #1 or Experiment #2 causes the most significant reduction in bubble sites. Wafers fabricated with these improvements are generally hermetic and survive HVZPM testing.

This study has shown how a previously un-reported technique of water electrolysis (bubble testing) can be used as an accelerated measurement method to evaluate circuit hermeticity and predict subsequent long-term humidity performance in less than one hour per wafer. Results presented here indicate that processing variables can be quickly evaluated. The electrolysis test can correctly identify fabrication recipes that result in enhanced humidity performance.

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