Process Development on 0.12-μm Gate E/D GaAs MESFETs with f_T and f_{max} > 100GHz Using Direct Ion Implantation for Low Power IC Applications

Z. Tang, H. Hsia, D. Becher, D Caruth, and M. Feng

Microelectronics Laboratory, Department of Electrical and Computer Engineering
University of Illinois, Urbana, IL 61801, USA
Phone: +1-217-333-4054, e-mail: ztang@hsic.ccsm.uiuc.edu

ABSTRACT

In this paper, the DC and RF characteristics of 0.12-μm gate E/D mode MESFETs have been presented. An f_T of 109 GHz and fmax of 126 GHz was achieved on E-mode MESFET and f_T of 105 GHz and fmax of 141 GHz on D-mode MESFET. This is the first reported E-mode GaAs MESFET using direct ion-implantation with f_T over 100GHz.

INTRODUCTION

Direct implanted GaAs MESFET has become the primary workhorse for high-speed and millimeter-wave wireless applications due to its high performance-cost ratio. The depletion-mode MESFET has demonstrated excellent device performance [1-2]. An f_T of 121GHz was reported on directed ion-implanted MESFETs using low temperature 0.12-μm T-gate process [3]. Meanwhile, f_T of 113 GHz and f_{max} of 132 GHz for 0.1-μm gate [4] and f_T of 168GHz for 0.06-μm gate [5] have been achieved using a self-aligned gate process. For high-speed, low power communication system and digital applications, enhancement-mode device is favorable due to its lower power consumption and higher transconductance at low bias condition. However, the implementation of high-performance enhancement-mode MESFETs in low power IC and DCFL logic falls far behind than that of D-mode MESFETs. For self-aligned E-mode MESFETs, a 0.3-μm gate process with Vth of 50 mV yielded f_T of 52 GHz and fmax of 75 GHz [6]. Although the self-aligned process with planar structures have produced high-performance D/E-mode MESFETs, the fabrication process is complicated compared with that of a blanket-implantation and recessed-gate structure. In addition, the self-aligned process requires a high-temperature gate process, therefore, the gate metal composition must be carefully chosen to retain its Schottky barrier characteristics.

In this work, we demonstrate a simple low-temperature T-gate process using a novel implantation schedule for high-performance direct ion-implanted GaAs E/D-mode MESFETs. The 0.12-μm gate-length D-mode MESFET shows a f_T of 105 GHz and fmax of 141 GHz, and a peak transconductance of 419 mS/mm at Vds = 1.5 V. With the same implantation schedule, we also fabricated, for the first time, the E-mode MESFET exhibiting f_T of 109 GHz and fmax of 126 GHz. The peak transconductance of 538 mS/mm was measured at Vds = 1 V. The excellent E-mode MESFET performance provides the possibility of implementing high-speed, low-cost, low power integrated circuits and digital circuits using direct ion-implanted GaAs MESFETs.

DEVICE FABRICATION

GaAs MESFETs with gate length of 0.12-μm were fabricated on LEC-grown 3-inch semi-insulating GaAs (100) wafers. To extend the use of ion-implanted material to gate length of less than 0.2-μm, the channel depth must be reduced. By reducing the channel depth, we also avoided the self-closing gate metallization problem and improved the transconductance and channel pinch-off at the same time. The n-type channel region for the MESFETs was formed by Si^{29} direct ion implantation at 40 kV and 20 kV, with doses of 7.5 x $10^{12}cm^2$ and 2 x 10^{13} cm^2 respectively. A p-type Be implantation was performed at 50 kV and 1.5 x 10^{12} cm^2 to improve the device pinch-off. Wafers were then activated by a capless anneal at 850 ^{0}C in an H_2/AsH_3 atmosphere.

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An isolation etch was performed to define the active region. Then AuGe/Ni/Au ohmic contacts are formed by thermal and e-beam evaporation. The 0.12-µm T-gate shown in Fig. 1a was defined by e-beam direct writing using a tri-layer resist structure (5% PMMA/ 8.5% P(MMA-MAA) / 4% PMMA) at 40 kV and 1 nA (Fig. 1b). The Ti/Pt/Au was evaporated after gate recess etch to form the T-gate.

RESULTS

Fig. 2 shows the excellent current-voltage characteristics of 0.12-µm D-mode and E-mode MESFETs with good pinch off behavior and no kink effects. The device transfer characteristics of transconductance and source-to-drain current are shown in Fig. 3. For the D-mode MESFET, a peak transconductance of 419 mS/mm was achieved at Vg = 0.2 V and Vds = 1.5 V. The maximum drain-to-source current is 576 mA/mm, and the device pinches at –1.18 V. For the E-mode MESFET, peak transconductance is 538 mS/mm at Vg = 0.8 V and Vds = 1 V, maximum current is 291 mA/mm, and the pinch off voltage is 46mV. Pinch off voltage was defined as Ids equals 1mA/mm. The microwave performance was measured using HP8510C from 250MHz to 40.25GHz. Cutoff frequencies, f_T and fmax, were determined by extrapolating |H21| and mag (U) in –20 dB/decade to the unity gain point as shown in Fig. 4. For the D-mode MESFET, f_T is 105 GHz and fmax is 141 GHz. Excellent RF performance, f_T of 109 GHz and fmax of 126 GHz, was achieved on the E-mode MESFET.

CONCLUSIONS

By optimizing the implant scheme and the gate process, we have successfully developed 0.12-µm 100 GHz ion-implanted E/D-mode MESFET process. High cut-off frequencies, f_T of 105 GHz and fmax of 141 GHz for D-mode MESFET, and f_T of 109 GHz and fmax of 126 GHz for E-mode MESFET were achieved. This is the first reported ion-implanted E-mode MESFET with f_T over 100 GHz. The excellent E-mode MESFET performance opens up the possibility of high-speed, low-cost digital logic applications and low power applications using ion-implanted MESFETs.

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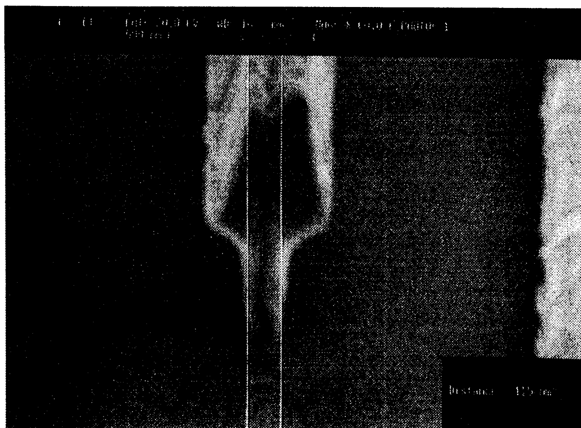
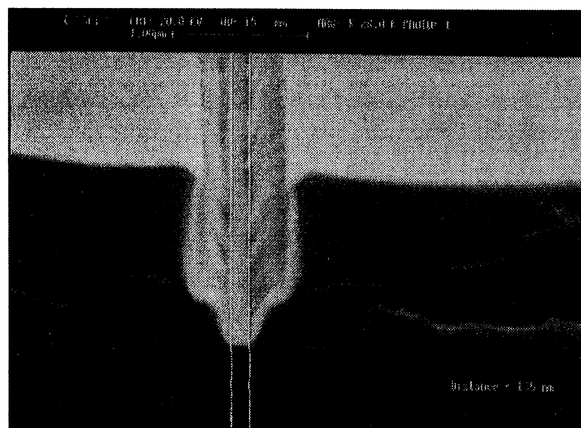


Fig.1 (a) Cross-section of 0.12-µm T-gate



(b) Tri-layer resist structure after development

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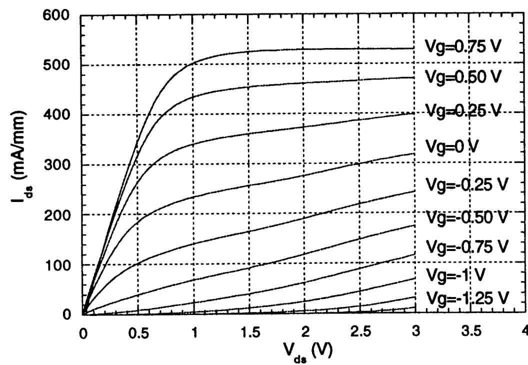


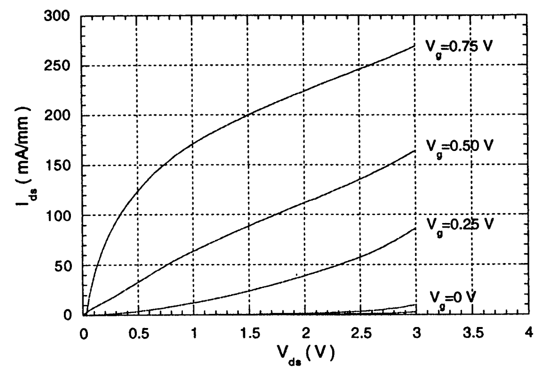
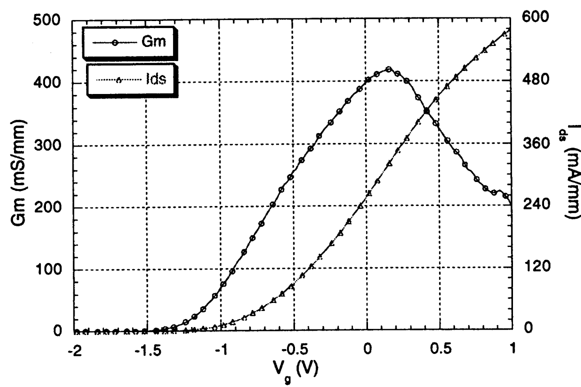


Fig. 2 (a) D-mode MESFET I-V Characteristics (b) E-mode MESFET I-V Characteristics



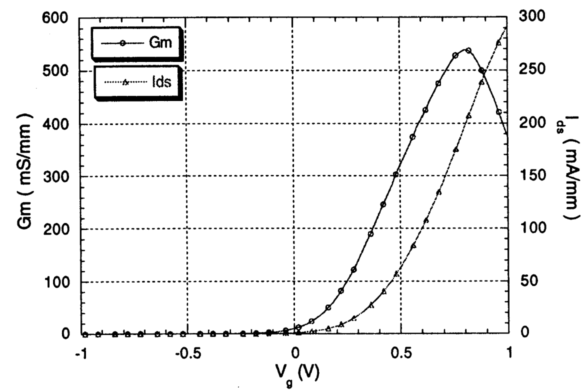
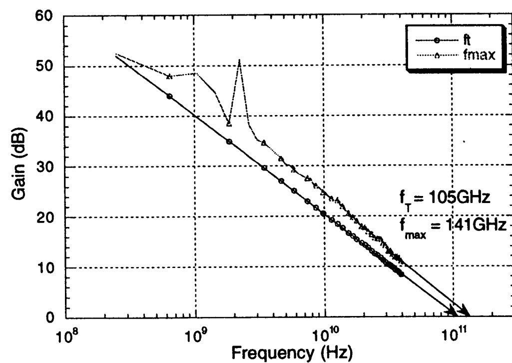


Fig. 3 (a) D-mode MESFET transfer characteristics (b) E-mode MESFET transfer characteristics



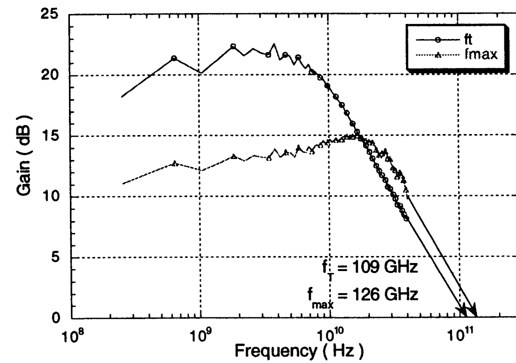


Fig. 4 (a) High frequency performance of D-mode MESFET (b) High frequency performance of E-mode MESFET

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