Cost Effective MeV Isolation Mask for Heterojunction Bipolar Transistors

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INTRODUCTION

Heterojunction Bipolar Transistors (HBTs) have become popular microwave power devices for commercial applications as well as military. Commercial vendors include cell phone manufacturers, future automotive electronics and satellite communication systems. They are attracted to HBTs for their superior power handling capabilities, high efficiency, single bias requirement as well as high linearity. The military's power requirements and need for high efficent devices for phased array radar, wide band electronic warfare (EW), communication systems and advanced power supplies generates the need for thicker collector structures. The load line for an HBT shows that for high power capability you need high voltage at low collector current and high current at low collector voltage. In order to increase the collector breakdown voltage for HBTs, the collector thickness should be increased. This increase in collector thickness will in turn raise the power capability for HBTs. Also, to reduce the extrinsic collector resistance thick sub-collectors are desirable for high frequency operation.

These requirements can make an HBT structure as thick as 3μm. By increasing the structure thickness, we introduce problems associated with fabrication of the device. Thick epitaxial layers make it difficult to isolate the device. Thicknesses of this magnitude make standard KeV implant technology marginally acceptable. There is typically a trade off in performance in order to maintain an acceptable structure thickness. If performance cannot be traded away, other options need to be considered.

BACKGROUND

There are three techniques typically used for HBT isolation:

1. Mesa Etch – etch off the entire structure
2. Partial mesa etch the structure and use KeV implantation
3. Use MeV implant technology.

By etching mesas the device becomes very non-planar and causes manufacturing difficulties with metal definitions and interconnects. Tall mesas require extra thick dielectric crossovers or very tall air-bridges. Figures 1 and 2 show the differences between the two techniques. Figure 1 is cross section of a 2 finger device processed with our planer thermal shunt process. Note how the shunt is planar across the device. The deepest etch is to the sub-collector layer. We are able to planarize using only one layer of polyimide.

However, in figure 2, you can see the extreme steps required to step over the mesas to connect the emitter to the isolated pads for a fully mesa process. For this process, air-bridges were used and required three layers of 1 μm thick Microlithography Chemical Corporation's NANO polymethylglutarimide (PMGI) to make the span.

Because of military requirements for high power applications which require thick epitaxial structures, Air Force Research Laboratory (AFRL) has chosen to use a planar MeV implant isolation approach[1]. The process uses the following implant schedule.

Oxygen	
Energ	Dose
(MeV)	(cm^{-2})
0.25	$8x10^{11}$
0.60	$1x10^{12}$
1.00	$1x10^{12}$
1.50	$1x10^{12}$
2.00	$5x10^{11}$
2.50	$1x10^{12}$
3.10	$5x10^{11}$
3.70	$1x10^{12}$
4.40	$5x10^{11}$
5.10	$1x10^{12}$
5.50	$1x10^{12}$

Table 1. Ion Implantation Schedule

In order to implant these energies, a robust masking scheme was needed. A traditional positive photoresist was first tried but was hardened by the high energy implant and was difficult to remove. Another mask was developed using a combination of photoresist and evaporated gold. Figure 3 shows a cross section of this mask. However, the process steps associated with this mask were not only time consuming, but very costly.

Due to the time and expense related to this process, most manufacturing facilities could not consider MeV isolation as a viable manufacturing process. It became necessary to develop a more cost effective process.

EXPERIMENT

PMGI resist was considered a possible candidate for a simplified mask. We use PMGI for our standard lift-off process and have found it to stick well to GaAs. Also, it is very hard, temperature tolerant, easily layered and has outstanding planarity over steps. It is also easily removed using a standard photoresist stripper. In order to determine the effectiveness of PMGI as an implant mask, we used a 5μm layer on one half of a 3 inch wafer and used our existing implant mask on the other side. This was meant to give a direct comparison, using both masks on the same wafer. It should be noted that PMGI is a deep UV sensitive photoresist. It is patterned using a Flood DUV source and standard i-line photoresist as the masking material. The exposed PMGI is developed with PMGI Developer 101. The i-line photoresist can be removed with acetone without affecting the PMGI.

The implant isolation process step follows emitter metal deposition. We typically have two emitter material Transmission Line Model (TLM) test patterns on our masks. One which uses emitter metal and one which uses base metal. The TLM test structure using base metal contacts had thinner resist over the TLM structure than the emitter metal contact TLM due to emitter metal deposition prior to the isolation mask step. (See Figure 3) This turned out to be advantageous in determining the needed thickness of PMGI resist. We were able to measure both TLM structures to determine if we were close to the correct resist thickness.

RESULTS

Figure 4 shows sheet resistance data for the emitter TLM using base metal contacts. Note, that the emitter layer is damaged after implant, using 5 μm PMGI resist on the right side of the wafer. The left side of the wafer using the standard implant mask shows undamaged emitter material. However, if we are to look at the emitter TLM pattern using emitter metal contacts we get a very different picture. Figure 5 displays emitter layer data from the same wafer using the emitter material TLM with emitter metal contact pads. This data shows no difference between mask types. These results made it clear the resist thickness was not quite enough. The emitter

metal was 1µm thick. That meant the resist could not have been more than 1µm thicker, but it stopped the implant from damaging the emitter material.

We then decided to try using a 6µm layer of PMGI, one 1µm layer and one 5µm layer. Figure 6 shows the results from two wafers grown together but processed with different implant masks. It should be noted there is little difference in the two wafer's emitter layer sheet resistances.

CONCLUSION

The advantages to thick HBT structures for many applications have been discussed. However, when these structures are used, problems arise with process capabilities. These thick structures require a new technique for isolation. The traditional mesa etch process, which works well for low power HBT devices, is not suited well for thick HBT structures.

We have previously demonstrated an isolation mask using resist capped with gold. This masking scheme is extremely expensive and time consuming. We have now demonstrated a cost effective masking technique using readily available photoresist. We have shown data using this mask comparing it to the more expensive technique. The data shows the mask is effective in stopping the oxygen ions from penetrating to the sensitive emitter cap layer. This process has reduced the time to prepare wafers for implant from over one day to merely a few hours. Also, the mask removal process was reduced from hours to minutes.

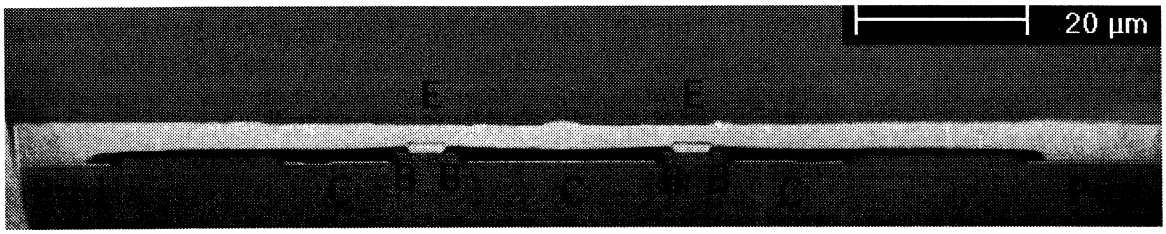

Figure 1. HBT cross section showing a polyimide planar process with MeV Implant isolation

Figure 2. HBT cross section showing a full mesa isolation process with air-bridge

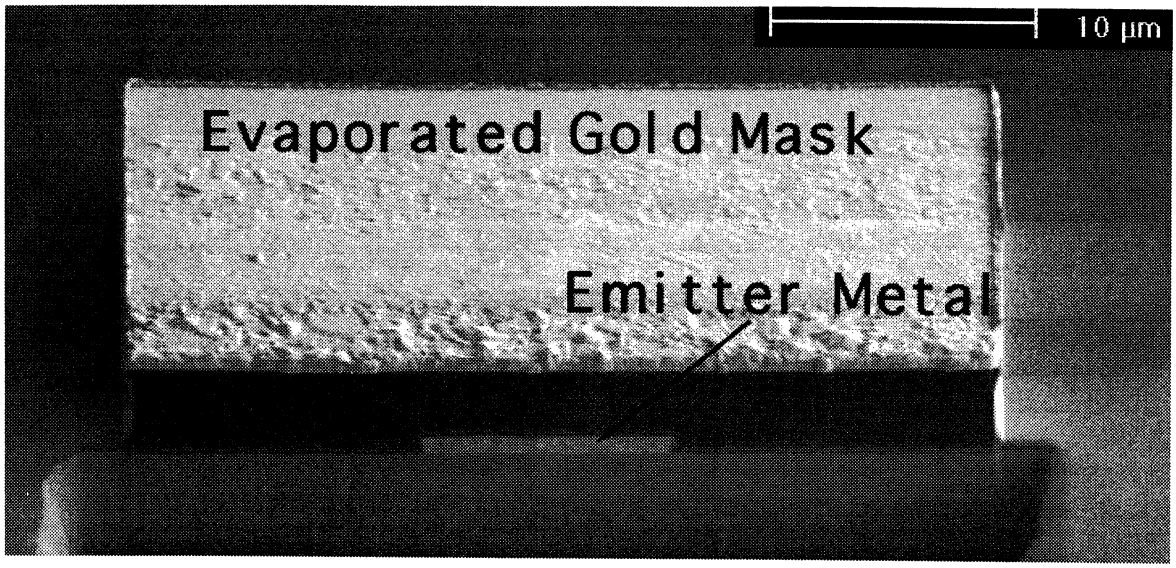

Figure 3. Original Implant Mask using photoresist and evaporated gold

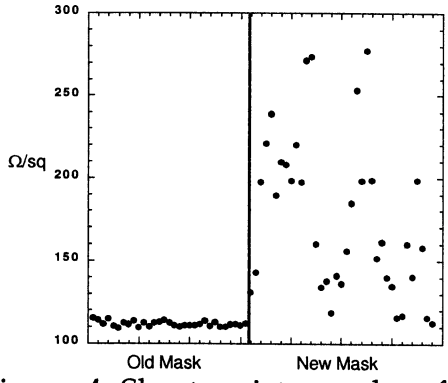

Figure 4. Sheet resistance data for the emitter TLM using base metal contacts

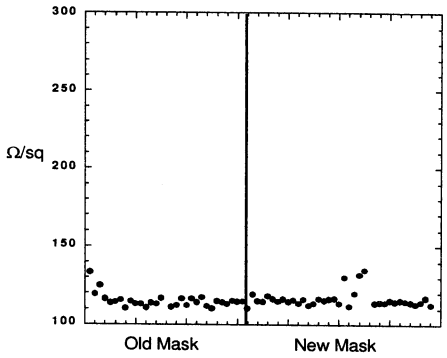

Figure 5. Sheet resistance data for the emitter TLM using Emitter metal contacts

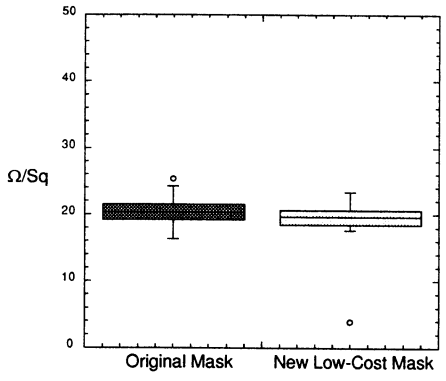

Figure 6. Emitter layer sheet resistances from sister wafers using, old and new masking schemes

[1] J Barrette, M. Mack, C. Bozada, R. Dettmer, R. Fitch, J. Sewell, T. Jenkins, A. McCormick. "Improved Oxygen Implant Isolation Process for Heterojunction Bipolar Transistors", *GaAs Manufacturing Technology*, 1995, pp 184-187.