Zero-Offset Low-Knee-Voltage GaInP/GaAs Collector-up Tunneling-Collector Heterojunction Bipolar Transistors for High-Efficiency High Power Amplifiers

K. Mochizuki*, R. J. Welty, and P. M. Asbeck

ECE Dept., University of California, San Diego, 9500 Gilman Drive, La Jolla, CA 92093-0407
*On leave from Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo 185-8601, Japan
Email: motizuki@ece.ucsd.edu, Phone: (858) 822-2285

C. R. Lutz, R. E. Welser, S. J. Whitney, and N. Pan

Kopin Corporation, 695 Myles Standish Blvd., Taunton, MA 02870

Abstract

We have developed a novel heterojunction bipolar transistor (HBT) structure, the collector-up tunneling-collector HBT (C-up TC-HBT), that minimizes the offset voltage $V_{CE,\,sat}$ and the knee voltage V_k. In this device, a thin GaInP layer is used at the base-collector junction to suppress hole injection into the collector. A collector-up structure is used because of the observed asymmetry of the band discontinuity between GaInP and GaAs depending on growth direction. Fabricated 120 x 120-µm² C-up TC-HBT's showed almost zero $V_{CE,\,sat}$ (5 to 10 mV) and a very small V_k of 0.34 V at 0.5 kA/cm², indicating that they are attractive candidates for high-efficiency high power amplifiers.

INTRODUCTION

GaInP/GaAs heterojunction bipolar transistors (HBT's) have become promising candidates for microwave high power amplifiers [1]. To improve their efficiency, particularly with low power supply voltage, it is important to reduce the offset voltage $V_{CE,\,sat}$ (value of collector-emitter voltage V_{CE} for zero collector current I_C) and the knee voltage V_k (the minimum value of V_{CE} at a given operating I_C). The value of $V_{CE,\,sat}$ is related to the difference between the base-emitter voltage V_{BE} associated with a given I_C, and the base-collector voltage V_{BC} associated with the same amount of forward current of the base-collector (BC) junction. The value of V_k is additionally affected by emitter and collector resistance, as well as voltage drops associated with any internal barriers.

One attractive method to increase V_{BC} at a given forward current (and thus reduce $V_{CE,\,sat}$) is to use a wide bandgap collector, such as GaInP. However, due to the resistance originating from the barrier for electrons at the BC junction, GaInP/GaAs double-heterojunction bipolar transistors (DHBT's) typically suffer from large V_k. For example, the V_k of large area transistors (2.9×10^{-5} to 1.4×10^{-2} µm²) at a collector current density J_C of 0.5 kA/cm² exceeds 1 V in reported results [2-6].

Another possible technique is to use a thin wide bandgap tunneling layer, which can prevent the flow of holes at the BC junction, although it can allow the flow of electrons. Since the function of such a structure is similar to that of the tunneling emitter bipolar transistor [7], the transistor can be called as the tunneling-collector HBT (TC-HBT). Considering the asymmetry of the band discontinuity between the interfaces of GaInP on GaAs and of GaAs on GaInP, which was observed in emitter-up and collector-up operation of GaInP/GaAs DHBT's [8, 9], the collector-up (C-up) configuration is expected to be better to achieve low $V_{CE,\,sat}$ and V_k of TC-HBT's. This configuration has a higher barrier for holes and a lower barrier for electrons at the BC junction.

Although C-up GaInP/GaAs HBT's were already reported by Girardot et al., their $V_{CE,\,sat}$ was high (0.625 V) because of the use of a thick GaInP etch-stop layer (18 nm) at the BC junction and Schottky collector contact [10]. In this work, we use a GaInP tunnel layer whose thickness is 10 nm to achieve low $V_{CE,\,sat}$ and V_k in C-up TC-HBT's. The use of such a thin tunnel layer is made possible by current advanced epitaxial growth technologies. The high etching selectivity between GaInP and GaAs is instrumental for reproducible fabrication.

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CHARACTERISTICS OF DIODES WITH AN INTERPOSED TUNNEL LAYER

We first investigated characteristics of n-on-p$^+$ and p$^+$-on-n GaAs diodes with an interposed GaInP tunnel layer. The epitaxial layer structure consists of a 600-nm-thick GaAs (Si: 5 x 10^{18} cm^{-3}) layer, a 600-nm-thick GaAs (Si: 1 x 10^{16} cm^{-3}) layer, a $Ga_{0.5}In_{0.5}P$ (Si: 5 x 10^{17} cm^{-3}) tunnel layer, a 70-nm-thick GaAs (C: 4 x 10^{19} cm^{-3}) layer, a $Ga_{0.5}In_{0.5}P$ (Si: 5 x 10^{17} cm^{-3}) tunnel layer, a 200-nm-thick GaAs (Si: 3 x 10^{17} cm^{-3}) layer, and cap layers of 100-nm-thick GaAs (Si: 5 x 10^{18} cm^{-3}) and 50-nm-thick $In_{0.5}Ga_{0.5}As$ (Si: 4 x 10^{19} cm^{-3}).

Forward current-voltage characteristics are shown in Fig. 1. Although all curves have a component with an ideality factor n of 2, they deviate from this slope at different current levels and at higher bias levels have a more ideal (n = 1) behavior. We consider that under the high bias condition, the shape of barrier for holes changes from trapezoid to rectangle, and the tunneling probability of holes rapidly decreases. To suppress n = 2 current, a 10-nm-thick GaInP layer was effective for n-on-p$^+$ diodes, while a thicker GaInP layer is required for p$^+$-on-n diodes. We attribute this difference to the asymmetry of the valence band discontinuity achieved during epitaxial growth [8, 9] and chose a C-up configuration with a 10-nm-thick GaInP tunnel layer.

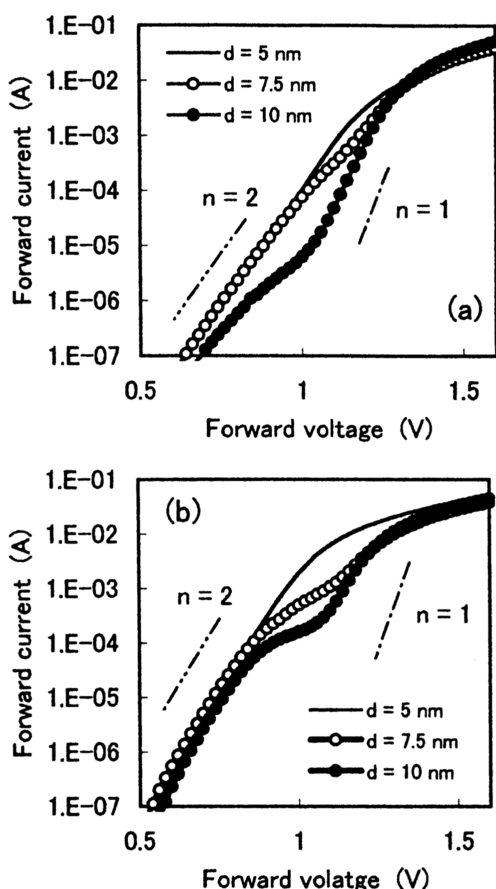

Fig. 1. Forward current-voltage characteristics of (a) n-type on p$^+$-type and (b) p$^+$-type on n-type GaAs diodes with an interposed GaInP tunnel layer. The area is (a) 100 x 100 μm^2 and (b) 110 x 210 μm^2. The thickness of the tunnel layer, d, was varied from 5 to 10 nm.

HBT FABRICATION

The C-up TC-HBT layer structure listed in Table I was grown on semi-insulating GaAs substrates by metal organic chemical vapor deposition. Transistors with a collector area S_C of 120 x 120 μm^2 were fabricated using a non-self-aligned process.

First, WSi was deposited on the InGaAs cap layer by RF sputtering and patterned into a nonalloyed collector electrode by reactive ion etching (RIE) using CF_4. Using this collector electrode as a mask, the InGaAs and GaAs cap layers were etched by wet chemical etching using a solution of $H_3PO_4 + H_2O_2 + H_2O$. The GaAs collector was then etched by RIE using CCl_2F_2. To make the extrinsic emitter highly resistive and suppress current flow in the extrinsic base-emitter junction region, a 2 x 10^{12}-cm^{-2} B ion implantation through the GaInP tunnel layer was carried out at 50 keV [10] [Fig. 2(a)].

TABLE I
EPITAXIAL LAYER STRUCTURE OF THE FABRICATED C-UP TC-HBT'S

Layer	Materials	Doping (cm^{-3})	Thickness (nm)
Cap1	n $In_{0.5}Ga_{0.5}As$	> 1 x 10^{19}	50
Cap2	n graded InGaAs	1 x 10^{19}	50
Cap3	n GaAs	5 x 10^{18}	50
Collector	n GaAs	3 x 10^{16}	600
Tunnel layer	n $Ga_{0.5}In_{0.5}P$	5 x 10^{17}	10
Spacer1	i GaAs		20
Base	p GaAs	3 x 10^{19}	70
Spacer2	i GaAs		5
Emitter	n $Ga_{0.5}In_{0.5}P$	5 x 10^{17}	100
Sub-emitter1	n $Ga_{0.5}In_{0.5}P$	2 x 10^{18}	150
Sub-emitter2	n GaAs	5 x 10^{18}	600

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Subsequently, a 0.35-μm-thick SiO_2 sidewall was formed by plasma-enhanced chemical vapor deposition and RIE etched using CHF_3. Using this sidewall as a mask, the GaInP tunnel layer, which should also act as a surface passivation layer of BC diodes [11], and undoped GaAs spacer layer were etched by wet chemical etching using solutions of HCl and $H_3PO_4 + H_2O_2 + H_2O$. This was followed by 10-min annealing at 390°C to decrease leakage in the boron-implanted extrinsic emitter [Fig. 2(b)].

Then, a Au/Ti base electrode was formed on the base layer by a liftoff technique. A base mesa was formed by wet chemical etching using solutions of H_3PO_4 + H_2O_2 + H_2O and HCl. Finally, a Au/Ni/Au/Ge emitter electrode was formed by a liftoff technique followed by alloying at 350°C for 20 sec [Fig. 2(c)].

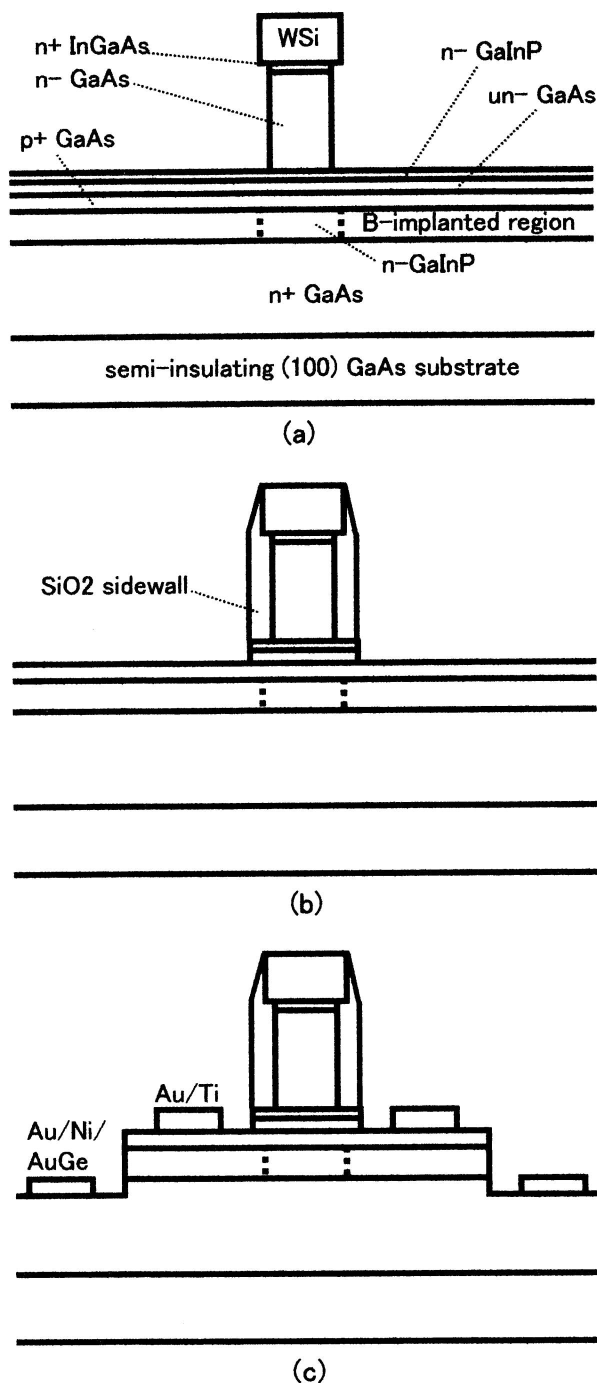

Fig. 2. Processing steps for the C-up TC-HBT.

HBT PERFORMANCE

DC performance of the fabricated C-up TC-HBT's was measured at room temperature using an HP 4155 curvetracer. The Gummel plot is shown in Fig. 3. The base leakage was less than 1 x 10^{-8} A for S_C = 120 x 120 μm^2. This leakage can be decreased further by optimizing the annealing condition after the ion implantation.

Figure 4 shows common-emitter current-voltage characteristics of the same transistor shown in Fig. 3. The current gain h_{fe} reached 50, which is higher than the value h_{fe} = 7 reported in C-up GaInP/GaAs HBT's [10]. A V_k of 0.34 V at 0.5 kA/cm^2 is much lower than those reported in DHBT's (V_k> 1 V) [2-6]. An extremely small $V_{CE,\ sat}$ of 5 to 10 mV was obtained due to the reduction of recombination current in the forward-biased BC diode, which came from preventing hole injection by the GaInP tunnel

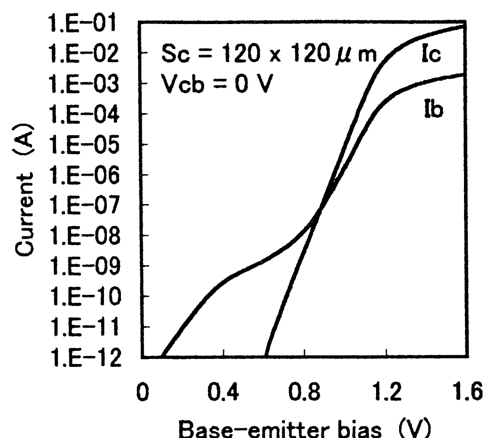

Fig. 3. Gummel plot of the fabricated 120 x 120-μm^2 C-up TC-HBT.

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layer. These characteristics make the C-up TC-HBT's attractive candidates for high-efficiency high power amplifiers.

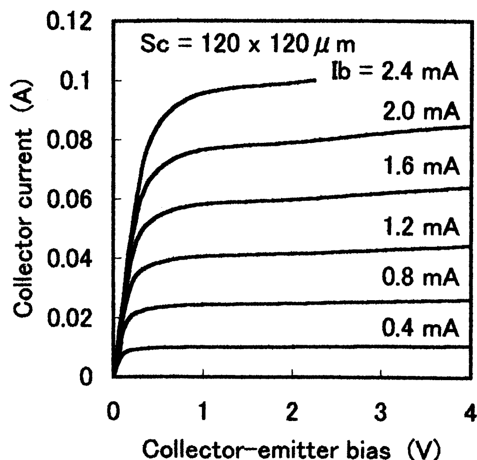

Fig. 4. Dependence of the collector current on the collector-emitter bias in the fabricated 120 x 120-μm² C-up TC-HBT.

CONCLUSIONS

We developed a novel C-up TC-HBT structure that minimizes $V_{CE,\,sat}$ and V_k. In this device, a 10-nm-thick GaInP layer was used at the BC junction to suppress hole injection into the collector. A C-up structure was used because of the observed asymmetry of the band discontinuity between GaInP and GaAs depending on growth direction. The fabricated C-up TC-HBT's showed almost zero $V_{CE,\,sat}$ (5 to 10 mV) and a very small V_k of 0.34 V at 0.5 kA/cm², indicating that they are attractive candidates for high-efficiency high power amplifiers.

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