Optimization of HIGFETs on LT-GaAs Buffer

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Abstract

The application of low temperature buffers in complementary HIGFET devices has been previously shown to improve the radiation hardness of HIGFET circuits [1] and enable good performing submicron P-channel devices and complementary circuits [2]. However significant degradation of N-channel FET performance is observed using the LT-buffers. This paper describes optimization of the LT-buffer to reduce the device degradation.

INTRODUCTION

Complementary GaAs (CGaAs™) technology has been developed in the last several years for low power, high speed digital circuits. With incorporation of low temperature GaAs buffers in the HIGFET epitaxial structure, submicron N and P-channel devices of gate lengths 0.3 um were realized with low subthreshold currents. Additionally, functional complementary HIGFET circuits of gate length 0.5 um with integration density as high as 60 K gates were demonstrated under Motorola's Celestri™ program. More recently, the focus of the technology is for RF applications. Low temperature buffers improved the pinch-off characteristics of P-HIGFETs and overall radiation hardness of CGaAs due to the short lifetime of photo carriers in the LT-buffer. Unfortunately, improving the P-channel device subthreshold current characteristics requires the LT-GaAs buffer to be placed close to the InGaAs channel which causes significant degradation of the N-channel device performance. Current density degradation of more than 100% were observed using a 5000 Å LT buffer with a 500 Å Al.75Ga.25As or AlAs undoped diffusion barrier and i-GaAs 1000 Å buffer separating the active InGaAs channel. The N-channel device degradation was curtailed by increasing the distance of the active channel from the LT buffer with corresponding increases of P-channel FET subthreshold leakage current. The cause of the N-channel FET degradation was increase of the source series resistance due to out-diffusion of point defects from the LT region despite the AlGaAs diffusion barrier. This paper discusses improvement of the low temperature buffer process by incorporating Be dopant in the LT region, to minimize outdiffusion of gallium vacancy traps from the LT into the active device.

LT-BUFFER HIGFET PROCESS

The standard CGaAs epitaxial structure without low temperature buffer and CGaAs process has been reported in the past [3,4]. The structure incorporating a normal low temperature GaAs buffer is shown here in Figure 1. Starting from an LEC GaAs substrate and a pre-conditioning GaAs layer, a low temperature GaAs layer 5000 Å is grown near 200 °C using MBE. An undoped AlGaAs layer of 500 Å is next grown near 600 °C and capped with a thin undoped GaAs. The structure is annealed at 600 °C for 10 mins in the MBE system under arsenic overpressure and subsequently the rest of the HIGFET structure consisting of 1000 Å undoped GaAs, a silicon delta doped GaAs, 30 Å GaAs spacer, 150 Å InGaAs channel, 250 Å AlGaAs insulator and a 30 Å GaAs cap grown at 600 °C.

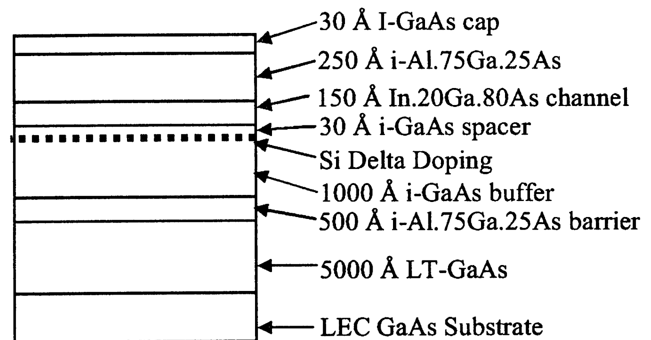

Figure 1. HIGFET epitaxial layer structure with low temperature (LT) buffer layer. The LT GaAs layer is capped with an $Al_{.75}Ga_{.25}As$ diffusion barrier.

Low temperature GaAs grown near 200 °C is non-stoichiometric and contains excess arsenic to the tune of 1-2%. Following the 600 °C anneal the excess arsenic precipitates out in the buffer. The point defects As_{Ga} and V_{Ga}, concentrations in the buffer depend on the growth temperature. Therefore to ensure reproducible levels of point defects, calibration of the temperature is important. An approach of selecting a thermocouple temperature resulting in a particular lattice constant of a coupon wafer was performed prior to growing the HIGFET wafers. The temperature corresponding to a lattice mismatch of the pre-anneal LT-GaAs of 1200 ppm relative to a 600 °C grown GaAs, was selected for growth. The lattice mismatch curves of different MBE systems used in the work were first derived. Figure 2 shows such curves for three vendors compared to results of two reference optical measurement methods. The MBE systems of PCRL, Vendor A and

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Vendor B used thermocouples for temperature measurement rather than an optical technique, such as diffuse reflectance spectroscopy which measures the bandgap of the GaAs epilayer.

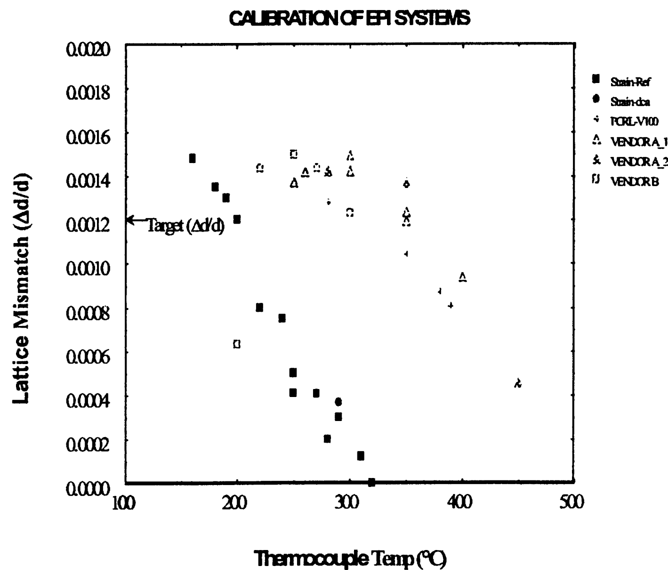

Figure 2. Calibration of growth temperature of LT-GaAs buffer for production MBE systems of different vendors. Since absolute thermocouple temperatures differ from system-to-system, a constant lattice mismatch difference of LT-GaAs and normal 600 °C grown GaAs was targeted.

HIGFET devices were fabricated using a refractory TiWN gate self-aligned by ion implantation process with refractory ohmics. Silicon was used for n-type self-aligned implant and F+/Be for both Ldd and contact implants of the PFET. Optimization of the implant anneal temperatures for low subthreshold currents have been previously reported [2].

P-type anneal temperature as low as 700 °C was used to contain subthreshold leakage currents to as low as 23 nA for 0.3 x 10 um PFETs.

BE-DOPED LT-GaAs BUFFER

The motivation for considering Be doping in the LT buffer was to reduce suspected gallium vacancy outdiffusion into the i-GaAs undoped buffer. N-type self-aligned implant sheet resistivity was found to be rather too high for NFETs with the LT structures, and had a large lot-to-lot variation, if the calibration approach discussed above were not used. The standard HIGFET without LT-buffer achieved a sheet resistivity of near 450 ohm/sq using a Nplus implant condition in the 10^{13} cm^{-2} range and anneal near 800 °C. The standard HIGFET uses 2000 Å of i-GaAs buffer and no LT buffer. Since the thickness of the i-GaAs buffer is reduced to 1000 Å in the LT structures, the sheet resistivity is expected to increase to about 520 ohms/sq. Figure 2 shows a simulated sheet resistivity of i-GaAs as function of thickness. In reality, the sheet resistivity on LT-buffers ranged from 600 ohms/sq to as high as 1270 ohms/sq and was vendor-to-vendor and lot-to-lot dependent. With the calibration approach discussed above, sheet resistivity consistently under 800 ohms /sq was achieved with all vendors.

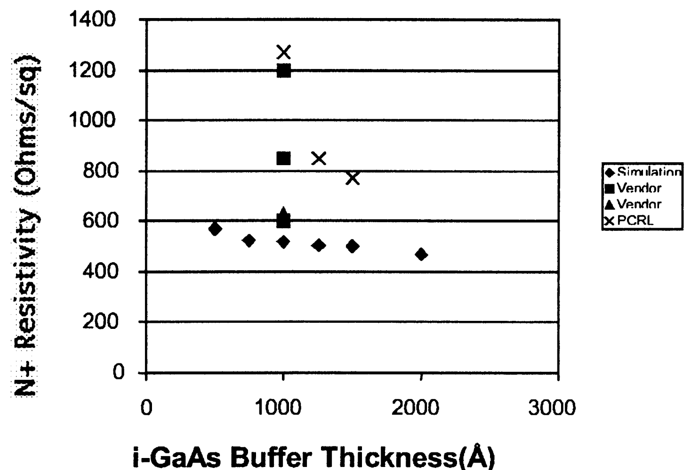

Figure 3. N+ implant sheet resistivity of HIGFET with normal 5000 Å LT buffer and 500 Å $Al_{.75}Ga_{.25}As$ diffusion barrier. The sheet resistivity of standard HIGFETs with no-LT was about 450 ohms/sq, very close to the simulated value using 2000 Å i-GaAs buffer. Lot-to-lot variation is shown by the data at 1000 Å I-GaAs buffer thickness.

The Be-doped LT buffer reported here was grown at 295 °C with Be concentration of 1e18 cm^{-3}. Sheet resistivity of the Be-doped LT GaAs was above 10^5 ohms/sq. Some wafers were grown with or without the undoped 500 Å AlGaAs diffusion barrier. The latter case resulted in significant increase (micro-ampere range) in P-channel FET subthreshold currents indicating outdiffusion of the Be doping into the i-GaAs buffer. However, with the 500 Å AlGaAs barrier, this diffusion was minimized resulting in PFET leakage current below a micro-amp. Based on the preliminary results, reduction of the Be doping to the 10^{17} range is expected to yield acceptable low P-channel subthreshold currents, below 100 nA. N-channel FET sheet resistivity near 600 ohms/sq was achieved and improvement of the N-channel FET drain current was realized.

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DEVICE RESULTS

Table 1 shows a comparison of device characteristics of a standard non-LT HIGFET of 0.5 um gate length compared to equivalent LT-buffered HIGFET with no Be doping. Drain current and beta are about 100% lower for the LT-buffered N-channel devices. The P-channel device of the non-LT HIGFET cannot pinch-off. It has significant subthresold leakage current whereas the LT-buffered device has good pinch-off with subthreshold slope of 97.8 mV/dec. Degradation of drain current and FET Beta was attributed to a higher source series resistance in the LT device. Notice that the low temperature GaAs also improves the substhreshold leakage current of the submicron n-channel FETs.

TABLE I
COMPLEMENTARY DEVICE DATA FOR STANDARD VRS LT-BUFFERED HIGFETS

PARAMETER	NON-LT CGAAS 0.5 UM NFET	NON-LT CGAAS 0.5 UM PFET	NORMAL LT-CGAAS 0.5 UM NFET	NORMAL LT-CGAAS 0.5 UM PFET
THRESHOLD VOLTAGE (V)	0.4 ± 0.037	ND	0.458 ±0.008	0.55 ±0.034
DRAIN CURRENT (MA/MM) @VGS=VDS=1.5 V	347 ± 122	78 ± 5.9	176.4±11.8	49.6±5.5
BETA (MA/V2MM)	407 ± 37	ND	253.9±16	77.2±7.2
SUBTHRESOLD SLOPE (MV/DEC)	151 ± 40.8	836 ± 339	83.4± 1	97.8±11.9

Figure 3 shows the drain current of 0.5 x 10 um N-channel HIGFET on LT buffer where the i-GaAs thickness is varied between 750 Å and 1200 Å. The thicker buffer results in the highest drain current due to lower source resistance. Figure 4 shows the corresponding P-channel device drain currents and subthreshold slope. The subthreshold leakage current of the PFET increases with thicker i-GaAs buffer and the slope is highest for the thickest GaAs buffer.

The results of incorporating Be doping during growth of the low temperature buffer is shown in Table 2. N-channel and P-channel drain currents, Beta and subthreshold currents are compared to the standard non-LT buffered HIGFETs. The drain current of both the N-channel and P-channel FETs are still lower than those of the standard non-LT buffered CGaAs wafers. However, the use of Be doping has improved the drain currents and Beta values of the devices compared to the results of standard LT-buffered HIGFETs.

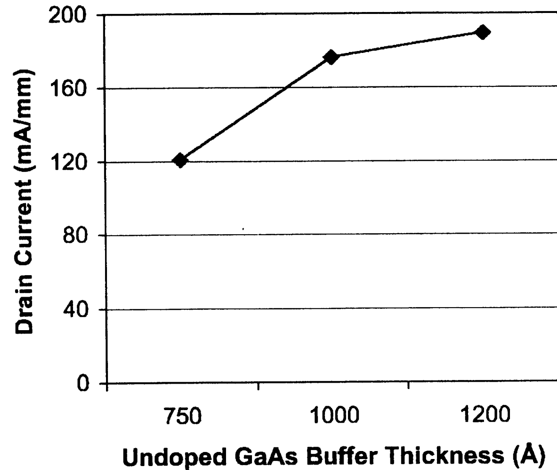

Figure 3. Drain current of 0.5 X 10 um N-channel HIGFET on LT-buffer versus the i-GaAs buffer thickness.

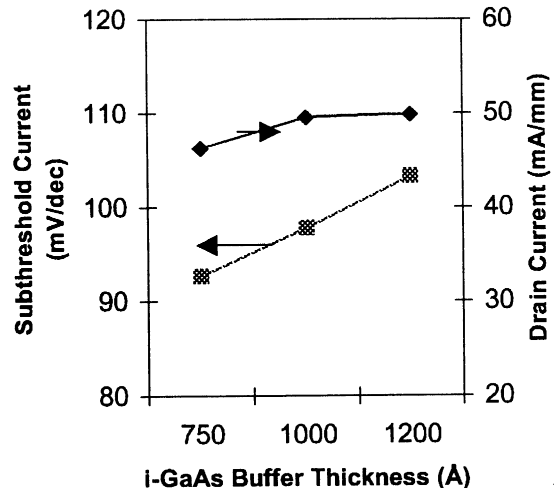

Figure 4. Drain current and Subthreshold Slope of 0.5 x 10 um P-channel HIGFET on LT-GaAs buffer

The concentration of Be in the LT GaAs was 1e18 cm^{-3} and the growth temperature of the LT GaAs was 295 °C using a thermocouple .
The subthreshold current of the P-channel devices were higher than the case without any Be doping, implying there is some outdiffusion of the Be dopant even though SIMs analysis indicated a sharp profile of the Be doping in the LT buffer. To check this, samples were grown without the AlGaAs difusion barrier.

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The subthreshold currents were found to increase significantly to several tens of micro-amperes making it difficult to pinch-off the devices. Thus, the level of Be doping must be carefully chosen to realize low subthreshold currents. We believe dropping the concentration to the 10^{17} per cm^{-2} range and ensuring a Be-doped LT-GaAs resistivity at least 10^{6} ohms/sq will enable lower subthreshold currents acceptable for high speed low power circuits (0.1 nA/um).

TABLE 2
COMPARISON OF STD NON-LT HIGFET AND BE-DOPED LT-HIGFET DC CHARACTERISTICS

PARAMETER	NON-LT CGAAS 0.5 UM NFET	NON-LT CGAAS 0.5 UM PFET	BE-DOPED LT-CGAAS 0.5 UM NFET	BE-DOPED LT-CGAAS 0.5 UM PFET
THRESHOLD VOLTAGE (V)	0.4 ± 0.037	ND	0.44 ±0.016	-0.458 ±0.056
DRAIN CURRENT (MA/MM) @VGS=VDS=1.5 V	347 ± 122	78 ± 5.9	191.7 ±43.5	54.5 ± 2.2
BETA (MA/V2MM)	407 ± 37	ND	297 ± 35.1	66.4±7.87
SUBTHRESOLD SLOPE (MV/DEC)	151 ± 40.8	836 ± 339	79.4 ± 4.16	300± 43.7

As noted in Table 2, the inclusion of Be doping in the LT-GaAs region has resulted in improved drain current and transistor Beta. The results in Table 2 correspond to 11 sites on the wafers. Beta values as high as 337 mA/V2mm and drain currents 225 mA/mm were measured on some sites. The improvement is due to reduction of trap impurities from the LT-region which resulted in improvement of the source resistance. The point defects, are considered to be gallium vacancies. The concentration of gallium vacancies in the LT-GaAs region is reduced by Be doping since Be sits on gallium sites in the LT-GaAs buffer. The amount of remaining vacancies migrating into the i-GaAs buffer is reduced. The diffusing defects were speculated as gallium vacancies. However with a high concentration of excess arsenic in the LT-buffer lattice, arsenic interstitials may also out-diffuse. The N-type sheet resistivity in the i-GaAs was always higher than the standard non-LT wafers indicating that any arsenic interstitial donors may not have affected the sheet resistivity of the silicon dopant

CONCLUSION

Complementary GaAs technology has been used for high speed low power circuits. Application of low temperature GaAs technology enabled submicron devices of gate lengths down to 0.3 um to be realized. 0.5 um CGaAs circuits with gate count as high as 60 K gates were found functional using the low temperature buffers. However, drain currents of particularly the N-channel device were found to be significantly degraded. For 0.5 um gate length devices, transistor drain currents and Beta dropped from their norminal values of 340 mA/mm and 407 ma/V2mm to 176 mA/mm and 223 mA/V2 mm respectively, at best. The i-GaAs buffer of reduced thickness 1000 Å compared to the standard buffer of the non-LT device (2000 Å) does not account for the whole increase in sheet resistivity of the implanted silicon source drain. Point defect diffusion through the AlGaAs barrier was considered the primary cause of the sheet resistivity and device performance degradation. Incorporation of Be doping in the LT buffer reduced the gallium vacancy concentration in the LT-buffers lowering the level of diffusion, and improving the device performance. Drain current and Beta of 225 mA/mm and 337 mA/V2mm were achieved on 0.5 um gate length devices.

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