

Utilization of Design of Experiments Combined with Technical Knowledge to Increase Manufacturability of a HIGFET Device

Eugene Huang and Mark R. Wilson

Motorola Semiconductor Products Sector
Compound Semiconductor One: CS-1
2100 E. Elliot Rd, Mail Drop EL609 Tempe, AZ 85284
Phone: (480)413-6370, FAX: (480)413-5748, Email: Eugene.Huang@motorola.com

ABSTRACT

Motorola has demonstrated a true enhancement heterostructure insulated-gate FET device (HIGFET). While transferring this technology to production, it became clear that several manufacturing issues needed to be resolved. One major obstacle was to increase breakdown voltage with repeatable results without sacrificing RF performance. Through SILVACO simulation software, it became clear that only the tail of the implant profile was residing in the channel region of the device, which resulted in a highly variable region of operation. Based on these results, several process areas were investigated. When attacking these elements independently or even two at a time, the goal of higher and more repeatable breakdown voltage was not achieved. As a result, a design of experiments (DOE) methodology was employed. The outcome was superior device performance.

I. INTRODUCTION

In the initial phases of development at Motorola, a plethora of device and process optimization was done to achieve a true enhancement mode RF power device that operated at 3.5 Volts at a frequency of 900 MHz [1]. However, as is the case a lot of times, when transferring this technology to full-blown production, several previously undetected manufacturing issues arose. One such issue was the inability to achieve a consistent, desired breakdown voltage from one lot to the next.

After several process parameters were identified for investigation, experiments looking at one or even two of the process parameters were run that would hopefully solve the problem. This turned out to be unsuccessful. A solution was reached only when a DOE methodology was incorporated. This paper will demonstrate in complete detail how a more manufacturable HIGFET was obtained through the integration of technical expertise combined with a DOE approach.

II. TECHNICAL EXPERTISE

After much discussion and experimentation, it became evident that the variation in breakdown voltage was caused by the fact that only the tail of the implant profile was being im-

planted in the channel layer of the HIGFET device. This hypothesis was further confirmed through the use of SILVACO simulation software. The current implant dose, implant energy, rapid thermal anneal conditions along with the epitaxial structure were inputted. Variations in implant energy were next simulated. With sheet resistance as the output variable (which correlates to breakdown voltage), simulation showed that the current process was in a highly sloped region, leading to the variability seen in breakdown voltage (See Fig. 1).

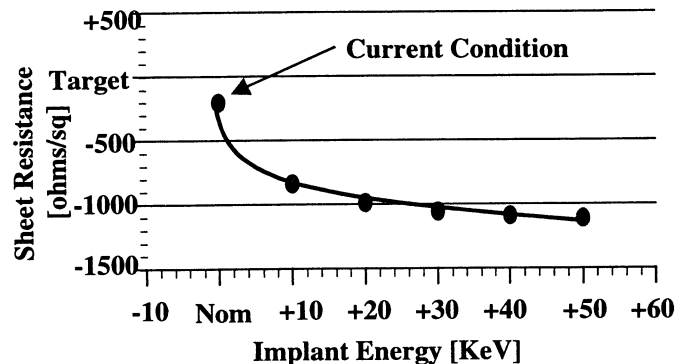


Fig. 1 SILVACO simulation showing that the current HIGFET process was in a highly sloped region thus confirming the hypothesis that only the tail of the implant profile was in the channel layer.

Based on this knowledge, it was determined that the process conditions that could potentially eliminate this variability were as follows: a) RTA time, b) RTA temperature, c) Implant dose and d) Implant energy. Thus, experiments looking at attacking the four factors independently or even two at a time were run. The result was that the goal of higher and more repeatable breakdown voltage was not achieved (See Fig. 2). Assuming the hypothesis that only the tail of the implant profile was in the channel layer, this meant that multi-factor interactions were most likely taking place. Only a well-designed DOE would be able to prove this theory out.

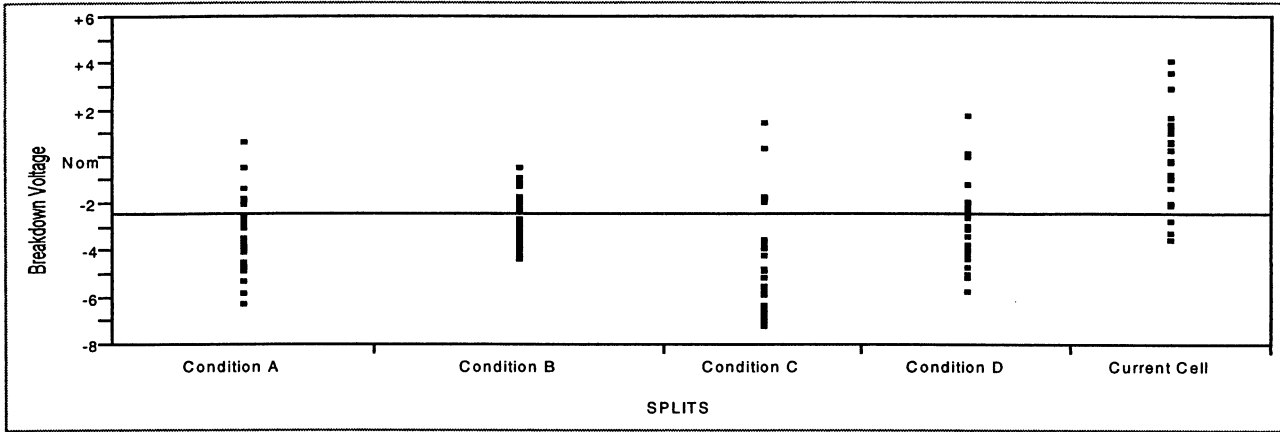


Fig. 2 Breakdown voltage versus different RTA, Implant conditions. The goal of obtaining higher and more repeatable breakdown voltage was not achieved when attacking the four factors independently or even two at a time. A well-designed DOE to look at multi-factor interactions was needed.

III. RESPONSE SURFACE METHOD (RSM) DOE

After it became clear that a design of experiments (DOE) approach was needed to obtain a more robust area of operation, the right DOE needed to be selected. There are many good sources of textbooks on the market which provide good insight into the design, modeling, and analysis of experiments [2,3]. A Response Surface Method (RSM) experiment was chosen since a starting point already existed. This would allow better exploration of the surface to determine an optimal place of operation. Within RSM, there are several designs one can choose. For this project, a Box-Behnken design was utilized.

The design encompassed the following four factors: a) Nominal RTA time ± 20 seconds, b) Nominal RTA temperature $\pm 20^\circ\text{C}$, c) Nominal Implant Dose $\pm 2e12$ and d) Nominal Implant energy $\pm 30\text{KeV}$ (See Table 1). As a sidenote, the current process settings were also included. A total of sixty wafers were used in this DOE.

After completion of the wafers through electrical test, JMP statistical software was used to model the results and to analyze the data. The model created was able to accurately predict the current process conditions as well as suggest a different region of operation which would give approximately 3.5 – 4.0 Volts higher breakdown voltage without detriment to other DC electrical parameters such as I_{dss} and V_{th} (See Fig 3). Based on these results the next step was to run an optimization DOE using the model predicted process conditions. This new set of RTA and implant process points would serve as the centerpoints in the optimization DOE. By doing this, it would map out the new process space to an even greater detail and “fine-tune” the process if needed.

Pattern	RTA		Implant	
	Time	Temp	Dose	Energy
--00	-	-	0	0
-+00	-	+	0	0
+000	+	-	0	0
++00	+	+	0	0
00--	0	0	-	-
00+0	0	0	-	+
00+0	0	0	+	-
00++	0	0	+	+
-00-	-	0	0	-
-00+	-	0	0	+
+00-	+	0	0	-
+00+	+	0	0	+
0-00	0	-	-	0
0-+0	0	-	+	0
0+00	0	+	-	0
0++0	0	+	+	0
-0-0	-	0	-	0
-0+0	-	0	+	0
+0-0	+	0	-	0
+0+0	+	0	+	0
0-0-	0	-	0	-
0-0+	0	-	0	+
0+0-	0	+	0	-
0+0+	0	+	0	+
0000	0	0	0	0
Curr	Curr	Curr	Curr	Curr

Table 1 The Box-Behnken RSM Design of Experiments. The four factors under investigation are as follows: a) RTA time , b) RTA temperature, c) Implant Dose and d) Implant Energy.

[0] = Nominal, [-] = Lower Bound, [+] = Upper Bound

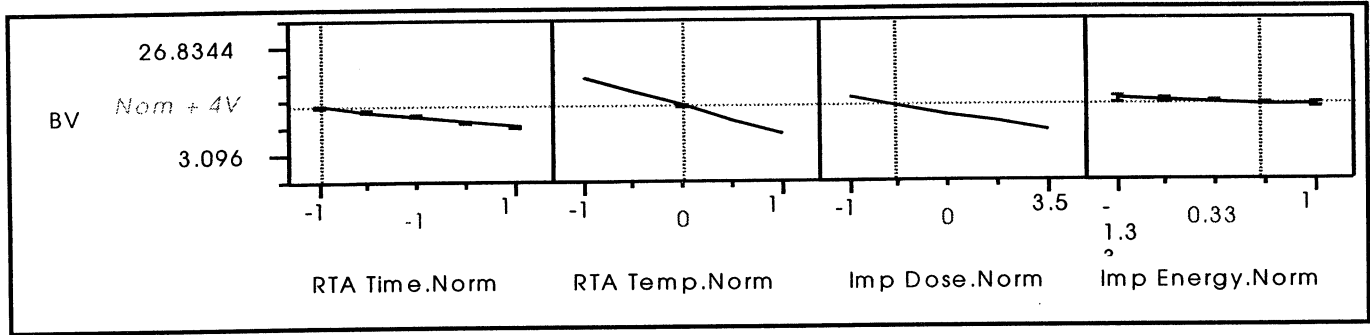


Fig. 3 Results of the Box-Behnken RSM Design of Experiments. JMP statistical software was used to model a new process space which would give 4V higher breakdown voltage without degradation in other DC electrical results.

IV. OPTIMIZATION DOE

The factors for the optimization DOE were varied as follows: a) Nominal RTA time ± 3 seconds, b) Nominal RTA temperature $\pm 20^\circ\text{C}$, c) Nominal Implant dose $\pm 0.5\text{e}12$ and d) Nominal Implant energy $\pm 10\text{KeV}$ (See Table 2). Again, the purpose was to explore the optimized process conditions in further detail and to determine if the chosen process parameters needed to be "adjusted". As it turns out, the implant dose was increased slightly to maintain maximum current, while breakdown voltage still rose by an average of 3.0-3.5 Volts.

V. CONCLUSIONS

Currently, additional lots are in line to ensure that with the new process conditions, consistent and higher breakdown voltage is indeed obtained over a span of time. Preliminary results from these lots do indeed support this. So in conclusion, this paper has demonstrated how a more manufacturable HIGFET device was obtained through the integration of technical "know-how" combined with a design of experiments approach. The benefits of exploring "process space" through DOE to achieve superior device performance were realized.

Pattern	RTA		Implant	
	Time	Temp	Dose	Energy
----	-	-	-	-
---+	-	-	-	+
--+-	-	-	+	-
--++	-	-	+	+
-+--	-	+	-	-
-++-	-	+	-	+
-+++	-	+	+	+
+---	+	-	-	-
++--	+	-	-	+
+++-	+	-	+	-
++++	+	-	+	+
+++-	+	+	-	-
+++-	+	+	-	+
+++-	+	+	+	-
++++	+	+	+	+
0000	0	0	0	0
Curr	Curr	Curr	Curr	Curr

Table 2 The Optimized Design of Experiments. The four factors under investigation are as follows: a) RTA time, b) RTA temperature, c) Implant Dose and d) Implant Energy.

[0] = Nominal, [-] = Lower Bound, [+] = Upper Bound

ACKNOWLEDGEMENTS

The author would like to thank Olin Harton who performed the Silvaco simulation, the transfer technology team led by Adolfo Reyes for fruitful discussions, and for the many individuals at CS1, Motorola's GaAs fabrication area, who diligently processed the many lot splits.

REFERENCES

- [1] J.H. Huang, E. Glass, J. Abrokwah, B. Bernhardt, M. Majerus, E. Spears, J.M. Parsey Jr., D. Scheitlin, R. Droopad, L.A. Mills, K. Hawthorne and J. Blaugh, "Device and Process Optimization for A Low Voltage Enhancement Mode Power Heterojunction FET for Portable Applications," IEEE GaAs IC Symposium Technical Digest, pp. 55-58, 1997.
- [2] Montgomery, Douglas C., "Design and Analysis of Experiments", John Wiley & Sons, 1991.
- [3] Box, George E.P., Hunter William G. and J. Stuart Hunter, "Statistics for Experimenters", John Wiley & Sons, 1978.