Device Characteristics of Dry Etched AlGaAs/InGaAs HEMTs Fabricated by Inductively Coupled Plasma Etching

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ABSTRACT

Passivated 0.2 μm pseudomorphic HEMTs (PHEMTs) were fabricated by combining a wide head T-shaped gate, formed by using a dose split method of electron beam lithography, with a short source-gate separation, formed by using an ICP dry recess etching process. The threshold voltages of the devices showed ±3% variation across three-inch wafers. The extrinsic transconductance and cutoff frequency of the PHEMT devices were 500 mS/mm and 82 GHz, respectively. The minimum noise figure of the PHEMT devices was observed around 80% of the saturation drain current at 30 GHz and V_{ds} = 2 V. The devices exhibited an F_{min} as low as 0.99 dB with an associated gain of 9.1 dB at 30 GHz. We have successfully fabricated 0.1 W power amplifier operating at 25.4 GHz operational frequency using the processes described above. We believe that the uniform device characteristics obtained across wafer are attributable to the gate recess etch process with the uniformity less than 3% achieved by using ICP technology.

INTRODUCTION

The parasitic gate resistance is one of the most important factors in determining noise performance of HEMT devices. In order to reduce the gate resistance, T-shaped gates with large cross-sectional area are required.[1][2] Also an asymmetric source and drain structure with shorter gate-source separation than gate-drain can be applied for reducing the source resistance using inductively coupled plasma (ICP) etching process. Wet chemical etching process of the gate area imposes difficulty to control etch uniformity, exact etch depth, and undercutting of the GaAs cap layer. Although conventional dry etch processes have good process controllability, it creates plasma damage. However, the ICP plasma dry etching technique creates much less damage due to the high plasma density with low DC bias.

In this study, we report the device characteristics of AlGaAs/InGaAs HEMTs fabricated by using a newly developed selective dry gate recess etch and wide head T-gate fabricated by using ICP etching and dose split electron beam lithography.

HEMT STRUCTURE AND FABRICATION

The AlGaAs/InGaAs PHEMT layers were grown by molecular beam epitaxy(MBE). They consist of 10 AlAs-GaAs superlattices, a GaAs buffer (600 nm), an $In_{0.15}Ga_{0.85}As$ channel sandwiched by planar Si doping layers (top; 5 × 10^{12} cm^{-2}, bottom; 2 × 10^{12} cm^{-2}), an $Al_{0.24}Ga_{0.76}As$ spacer, an $Al_{0.24}Ga_{0.76}As$ Schottky (30 nm), and n^+ GaAs cap layer (50 nm, 5 × 10^{18} cm^{-3}). The sheet carrier density of 2 DEG and the electron mobility measured at room temperature were 3.5 × 10^{12} cm^{-2} and > 6,100 cm^2/V·s, respectively.

To obtain low source resistance and reproducible gate recess processing, the n^+ GaAs cap layer was selectively etched using ICP dry etching using Oxford Plasma Technology Plasmalab System100™ as shown in Figure 1.

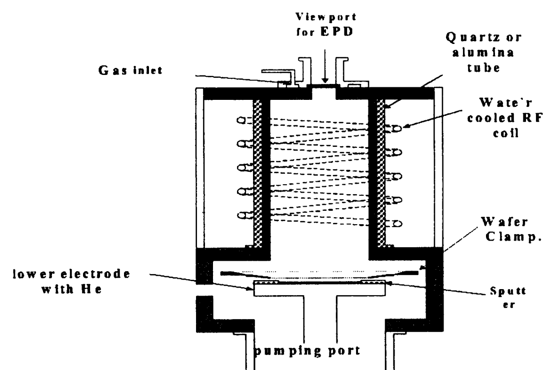

Figure 1. Conceptual diagram of inductively coupled plasma dry etch system.

The cap GaAs layer was selectively etched to the AlGaAs layer using an SF_6 and BCl_3 gas mixture, with bias voltage of less than 30V. The etch rate of GaAs cap layer and the etch selectivity of GaAs to AlGaAs were controlled to 1,000Å/min and 100, respectively. Etch uniformity was less than 3% on 3 inch wafer. The T-shaped gate electrode with a dose-split method (DSM) has been also used to reduce the gate resistance.[2] Those patterns were exposed by E-beam direct

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writing system with 45 kV acceleration voltage. The T-shaped gate formed by DSM has the ratio of gate head length to gate footprint larger than 10, which is higher than twice as that of the conventional T-shaped gate. Figure 2 shows a planar view of a HEMT device in which two single gates of 0.2 μm gate length and a unit gate width of 50 μm are connected in parallel. The drain electrodes are connected with Au-plated airbridges. The sequence for device fabrication is as follows. After mesa isolation by wet chemical etching in H_3PO_4: H_2O_2: H_2O = 4: 1: 90, ohmic contacts were formed by evaporating Ni/Ge/Au/Ti/Au metallic layers, and then alloyed at 410°C using a rapid thermal annealing. T-gate process using DSM with two-layer resists systems was developed to form a wide head T-shaped gate having large cross-sectional gate head on the fine gate footprint.[2] The exposure dose patterns and resist development conditions were optimized to form the short gate footprint reproducibly. The top and bottom resists were developed using a mixed solution of MIBK and IPA. The overhang of the top resist was suitable for the subsequent lift-off process.

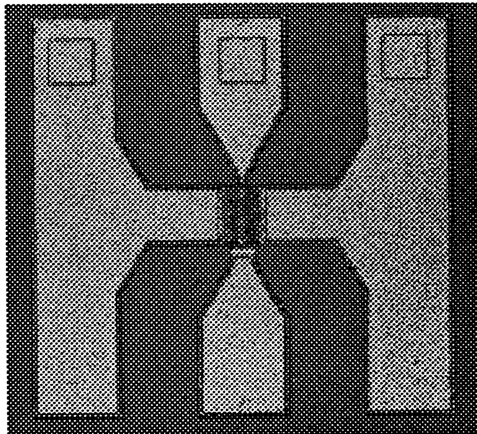

Figure 2. Plan view of InGaAs channel PHEMT device with two gates(0.2 μm gate length x 50 μm gate width) in parallel.

All of the recess etching was performed in an automatically loaded, load-lock ICP plasma etch system (Plasmalab system 100™) utilizing a 13.56 MHz excitation source with an additional RF (13.56 MHz) substrate biasing. The gate recess of GaAs PHEMT requires high selectivity of GaAs over AlGaAs. Recently, BCl_3/SF_6 gas mixture has been widely used for this purpose. It is well known that BCl_3 is used to etch both AlGaAs and GaAs and the role of SF_6 is to provide F^- radicals that react with AlGaAs and form AlF_3.

Since the boiling point of AlF_3 is high(~1291℃), it is a nonvolatile. Therefore, the etch rate of AlGaAs using BCl_3/SF_6 is low(<10 Å/min).[3][4] Figure 3 shows the etch rates of GaAs and AlGaAs with respect to SF_6 flow rate with BCl_3 flow rate fixed in the gas mixture at 100 W microwave power and -20 V self-dc bias. Etch rate of GaAs is increased

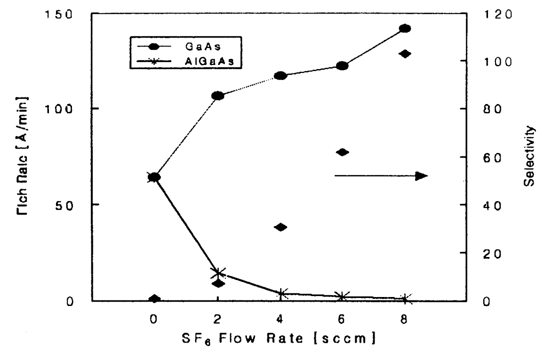

Figure 3. Etch rates of GaAs and AlGaAs and etch selectivity of GaAs to AlGaAs as a function of SF_6 gas flow rate.

with SF_6 flow rate, but that of AlGaAs is nearly constant. This result suggests that etch stop in AlGaAs layer is achieved by AlF_3 formation as observed by others.[3][4] From these results, we selected $9BCl_3/3SF_6$ mixture for gate recess. This gate recess etching process had no undercutting using BCl_3/SF_6 gas mixtures. In comparison, wet recess etching process using citric acid resulted in the lateral etch width of 0.05 μm in 0.2 μm gate pattern. For 0.5 μm source- gate separation, source resistance was improved by 10 % by using ICP etching compared to wet recess process. In a device with 100 μm width, the source resistance was 0.67 ohm. Figure 3 also shows that the etch selectivity of GaAs to AlGaAs increases with SF_6 flow rate, as also shown in Fig. 3. On the other hand, the etch rate of AlGaAs layer decreases with the SF_6 flow rate and becomes almost negligible compared to that of GaAs. It seems that the nonvolatile AlF_3 inhibiting layer was formed during etching process to result in the etch stop on the AlGaAs surface.

Figure 4 shows the etch selectivity of GaAs to AlGaAs with chamber pressure at constant RF power.(Note the scale difference between left and right ordinate.) As the etch rate of AlGaAs layer decreased with the chamber pressure, we obtained the maximum etch selectivity of GaAs layer to AlGaAs layer at a chamber pressure of 7 mTorr. At 15 mTorr, RF power suddenly decreased and the etch rate of GaAs layer suddenly decreased. This seems to be due to the significant scattering within the plasma that acts to obstruct the further etching reaction of GaAs to proceed.

After selective gate recess, Ti/Pt/Au (0.6 μm thick) layers were deposited and lifted-off. A wide head T-shaped gate formed by DSM exhibited large cross-sectional area having the aspect ratio of gate head length (1.15 μm) to gate footprint (0.2μm) larger than 7. After opening the contact windows for posts of the airbridge by reactive ion etch(RIE) process, the airbridges are formed by using a two-mask level process and electroplating to a final gold thickness. Finally, the device was passivated with Si_xN_y layer deposited by using plasma enhanced chemical vapor deposition(PECVD) system.

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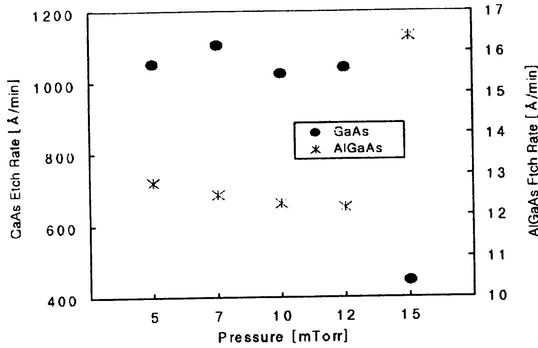

Figure 4. The etch selectivity of GaAs to AlGaAs with respect to chamber pressure at constant RF power.

DEVICE CHARACTERISTICS

Figure 5 shows the uniformity of transconductance and threshold voltage for the fully passivated $Al_{0.24}Ga_{0.76}As/In_{0.15}Ga_{0.85}As$ PHEMT devices with wide head T-shaped two finger gates of 0.2 µm length x 100 µm width. PHEMT devices exhibit excellent dc and pinch-off characteristics. The drain saturation current, I_{dss}, measured at V_{ds} = 2 V and V_{gs} = 0 V is 10 mA. This device has a gate-to-drain breakdown voltage of -9 V at 1mA/mm of gate current.

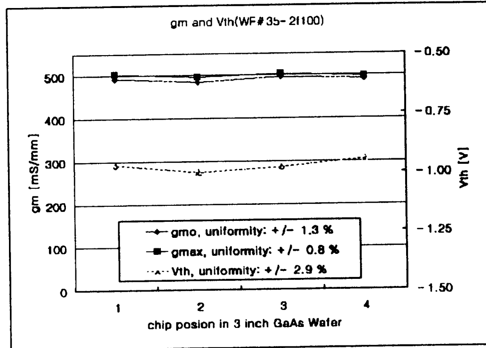

Figure 5. The uniformity of transconductance and threshold voltage of 0.2 µm length x 100 µm width gate PHEMT devices in a three inch wafer.

The variation of threshold voltage is within ±0.05 V. The threshold voltage, V_{th}, was -1 V measured at V_{ds} = 2 V. The maximum extrinsic transconductance, gm, measured at V_{gs} = 0.05 V and V_{ds} = 2 V was 500 mS/mm. The threshold voltage uniformity of PHEMT devices in a three inch wafer was less than 3%.

The s-parameters for the fabricated HEMTs were measured on a wafer from 1 to 50 GHz using a Cascade microwave probe station and an HP8510B network analyzer. Typical current gain, $|h_{21}|$, as a function of frequency for 0.2 x 100 μm^2 PHEMT devices is shown in Figure 6. The cut-off frequency, f_T, was obtained from the extrapolation of the $|h_{21}|$ to unity using a -6 dB/octave slope and the maximum frequency of oscillation, f_{max}, was extracted from small signal parameters. The f_T and f_{max} obtained for 0.2 µm x 100 µm gate PHEMT devices were 82.6 and 250 GHz, respectively.

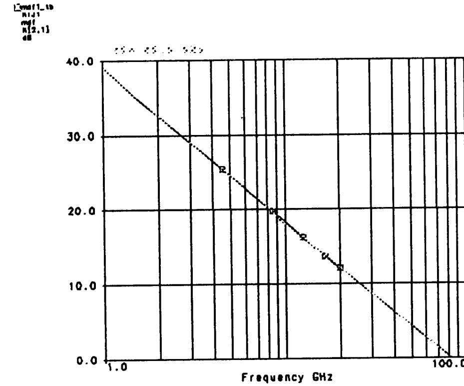

Figure 6. Typical current gain, $|h_{21}|$, as a function of frequency for 0.2 µm x 100 µm PHEMT with a wide head T-shaped gate.

Figure 7 shows Minimum noise figure and associated gain as a function of frequency. Noise figure measurements have been carried out in the frequency range between 2 GHz and 40 GHz by using an HP 8510B network analyzer,

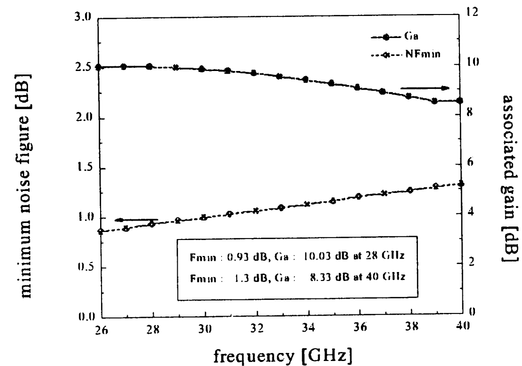

Figure 7. Minimum noise figure and associated gain as a function of frequency measured from 30 to 40 GHz at V_{ds} = 2 V and I_{ds} = 80 % I_{dss} (I_{dss} = 13 mA) for 0.2 µm x 100 µm PHEMT with a wide head T-shaped gate.

HP 8970B noise figure meter, and an ATN NP5 noise parameter test set. After each calibration routine (LRM ISS and SOLT), the same low-noise HEMT device has been tested at a fixed biasing condition (V_{ds} = 2.0 V, I_{ds} = 13 mA). The calibration data of the minimum noise figure, F_{min}, was within ±0.02 dB up to 40 GHz. At 12 GHz and V_{ds} = 2 V, the lowest F_{min} was observed around 70 to 80 % I_{dss} for the fully

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passivated 0.2 μm x 100 μm gate PHEMT device. Figure 7 exhibits F_{min} and the associated gain, G_a, as a function of frequency measured at 80% I_{dss} (13mA) and V_{ds} = 2 V for PHEMT device. The F_{min} measured at 30 GHz, including passivation loss with this bias condition (V_{ds} = 2 V, I_{ds} = 13 mA) is 0.99 dB with associated gain of 9.91 dB. At 40 GHz, F_{min} is 1.3 dB with G_a of 8.33 dB.

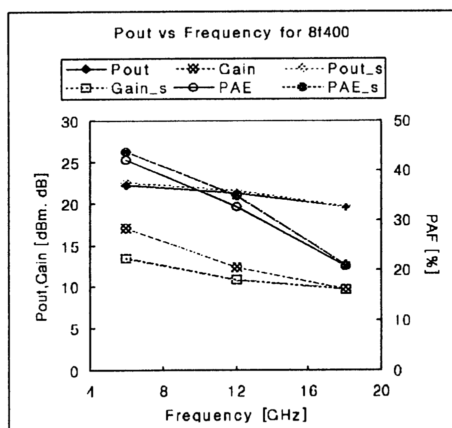

Figure 8. The output power with frequency of a HEMT device with 100 μm gate width.

Figure 8 shows the output power, P_{out}, with respect to frequency of the HEMT device with 0.2 x 100 μm^2 gate. P_{out} at P1dB and the gain of 100 μm-wide gate were 13.6 dBm and 9.28 dB at 18 GHz, respectively. The power added efficiency, PAE, was 18.3%. P_{out} at P1dB and the gain of 200 μm-wide gate were 18.89 dBm and 10.78dB at 18 GHz, respectively, and PAE was 27.3%. The largest PAE of the 400 μm device was 45.6% at 6 GHz. The PAE increased with gate width. The output powers at 18 and 12 GHz were 19.59 and 21.94 dBm with the power gains of 9.93 and 10.81dB, respectively.

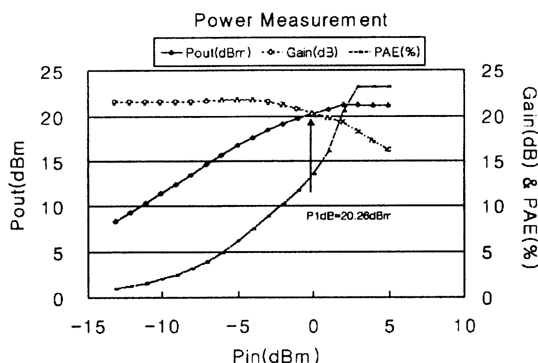

Figure 9. The output power results of a power amplifier with power level of 0.1W at 25.4 GHz.

Figure 9 shows P_{out} of power amplifier with power level of 0.1W at 25.4 GHz. As shown in Figure 9, P_{out} of MMIC was 20.3 dBm measured at 1 dB compression point. The power gain was 21 dB, and PAE at saturation output power was 23% and 13.5% at P1dB.

CONCLUSION

In this study, we have developed a fully passivated AlGaAs/InGaAs/GaAs PHEMT which combines a wide head T-shaped 0.2 μm gate fabricated by a dose split method of electron beam lithography with 0.5 μm separation of the source-gate contacts and an ICP dry recess etching process. The average threshold voltage of the devices was −1 V with 50 mV variation in a three inch wafer. The extrinsic transconductance and the cutoff frequency of fabricated PHEMT devices were 500 mS/mm and 82 GHz, respectively. The PHEMT device has shown the lowest minimum noise figure at around 80% of the saturation drain current for 30 GHz and V_{ds} = 2 V. This device exhibited very low noise figures of 0.99 and 1.3 dB at 30 GHz and 40 GHz, respectively. These values are among the lowest ones ever reported for the passivated PHEMTs with the same gate length and two-finger gate structure fabricated by using dry recess process. This was due to the extremely low source and gate resistances achieved by applying the wide head T-shaped gate and the short source-gate separation. We have also successfully demonstrated a 0.1 W power amplifier operating at 30 GHz using the processes described above. We believe that the uniform device characteristics obtained across wafer are attributable to the uniform gate recess etch process with the uniformity <3% achieved by using ICP technology.

ACKNOWLEDGMENT

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