

GaN Electronic Devices for Microwave Power Applications

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ABSTRACT

The dc, small-signal, and microwave power output characteristics of AlGaN/GaN HEMTs are presented. HEMTs with maximum drain current greater than 1 A/mm, gate-drain breakdown over 80V, and f_T of 30 GHz for a 0.4 μm gate have been demonstrated. Trapping effects, related to both surface and buffer layers, that limit device power performance are discussed. At 3.8 GHz, a CW power density of 3.1 W/mm and a pulsed power density of 5.9 W/mm have been achieved.

INTRODUCTION

GaN-based microwave power transistors have set the state-of-the art for output power density [1] and have the potential to replace GaAs-based transistors for a number of high-power applications. This material system, consisting of GaN, AlN, InN and their alloys, has become the basis of an advanced, microwave-power-device technology for a number of reasons. GaN has a high breakdown field, estimated to be 3 MV/cm, ten times that of Si or GaAs. It is these high breakdown fields that have made GaN an attractive material for the design of high-power devices. For microwave operation, a high electron velocity is required, and GaN fulfills this requirement with its high peak velocity of 3×10^7 cm/s. An additional characteristic distinguishes GaN from other wide bandgap semiconductors and that is the ability to make heterostructure devices that support a high carrier density with high mobility. As a result of these properties, excellent high-frequency, high-power device performance has been achieved with GaN-based HEMTs.

Much developmental work is still required, however. Due to the relative immaturity of the GaN technology, a variety of trapping effects have been noted. These include current collapse in the drain characteristics, gate- and drain-lag transients, transconductance frequency dispersion, light sensitivity, and restricted microwave power output. Extensive efforts directed toward an understanding and elimination of these trapping effects are currently underway. This parallels the development of GaAs-based microwave field-effect transistors, where significant attention was directed toward the minimization of trapping effects. In this paper the dc, small-signal, gate- and drain-lag, and microwave power output characteristics of GaN-based field-effect transistors will be presented.

MATERIALS GROWTH AND DEVICE FABRICATION

The device cross section is shown in Fig. 1. Devices with source-drain spacings of 2 to 6 μm and gate lengths of 0.2 to 2 μm were fabricated. The ohmic contacts are Ti/Al/Ni/Au and had a contact resistance in the range of 1-2 $\Omega\text{-mm}$. The gate metallization is Pt/Au and the devices were isolated with ion-implantation-induced damage. The epitaxial layers used in this work were grown by MOCVD. The AlGaN/GaN HEMT structures consisted of a 3 μm thick undoped, high-resistivity GaN buffer layer grown on top of a thin (200 \AA) low-temperature AlN nucleation layer. The thick buffer layer was employed to spatially remove the active part of the device from the higher-defect-density material near the substrate interface. An AlGaN layer with a nominal thickness of 300 \AA and a nominal Al composition of 30% was grown on top of the GaN buffer. Devices with and without Si doping in the AlGaN layer were studied.

DC CHARACTERISTICS

The output characteristics of several 50 μm wide devices from one GaN HEMT wafer are shown in Fig. 2. Maximum drain currents (at a forward gate current of 1 mA/mm) of ~ 1 A/mm are obtained. Somewhat higher currents are measured for tighter source-drain spacings. The maximum transconductance is ~ 220 mS/mm. The following Hall

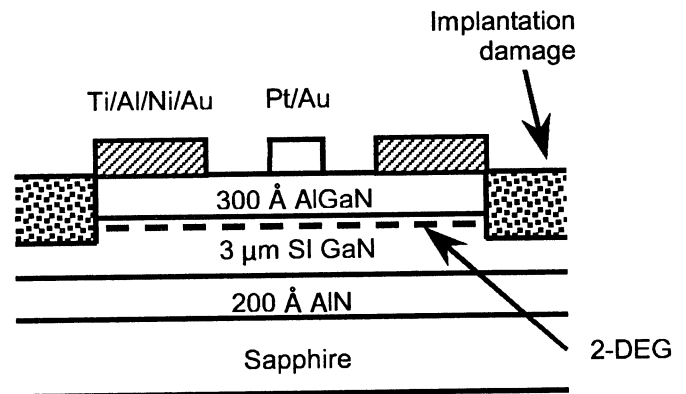


Fig. 1. GaN HEMT cross section.

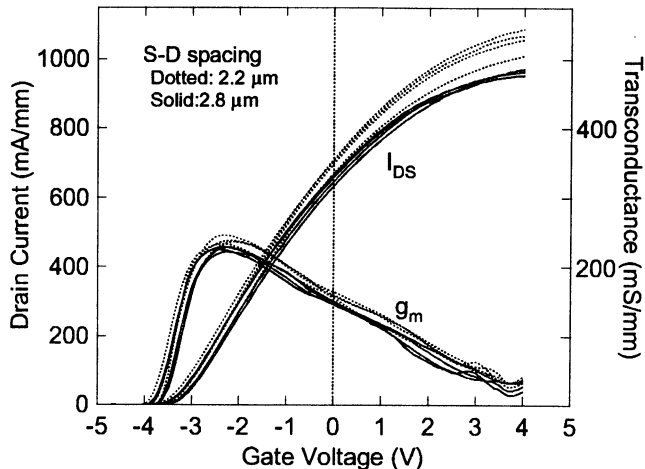


Fig. 2. Device output characteristics for several devices with $V_{DS} = 8$ V.

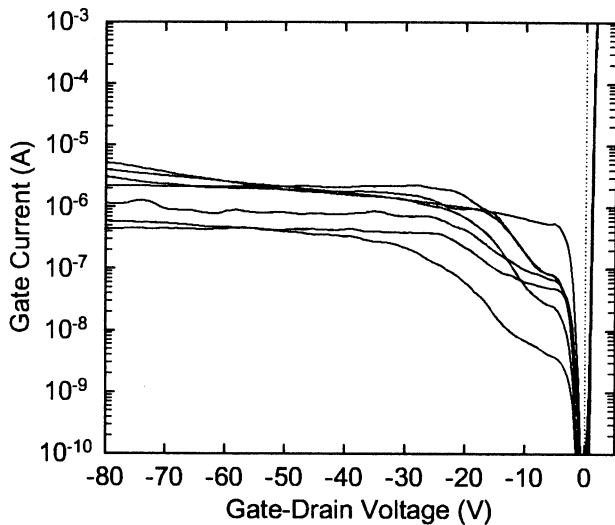


Fig. 3. Gate-drain I-V characteristics for several devices.

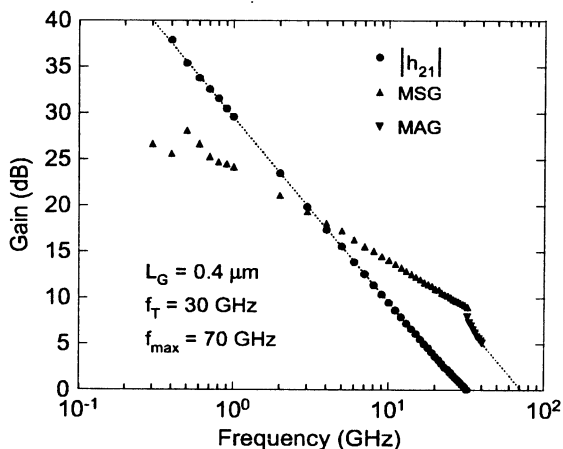


Fig. 4. Short-circuit current gain, maximum stable gain, and maximum available gain derived from measured S-parameters.

properties were determined for this wafer from on-wafer test patterns: a sheet resistance of $490 \Omega/\square$, a mobility of $1460 \text{ cm}^2/\text{V-s}$, and a sheet charge concentration of $8.8 \times 10^{12} \text{ cm}^{-2}$. The gate-drain breakdown voltage is in excess of -80V , as shown in Fig. 3. The ability to have a high channel current and at the same time a very large gate breakdown voltage is one of the clear advantages of the GaN technology.

SMALL-SIGNAL PERFORMANCE

The S-parameters of these devices were measured as a function of frequency and bias using on-wafer probing. The corresponding current gain, $|h_{21}|$, maximum stable gain, MSG, and maximum available gain, MAG, are given as a function of frequency in Fig. 4 for a $0.4 \mu\text{m}$ gate length. The usual 6 dB/octave curve fitting yields f_T and f_{max} values of 30 and 70 GHz, respectively. In Fig. 5, representative f_T values are plotted as a function of gate length for NRL devices as well as that reported by other organizations. It can be seen that the GaN HEMT high-frequency performance is comparable to that of GaAs MESFETs.

DRAIN CURRENT TRANSIENTS: DRAIN LAG

Representative drain characteristics are shown in Fig. 6. In this figure, two sets of characteristics are shown. The characteristics indicated by the dotted lines are the result when the maximum drain voltage is restricted to 5V, whereas the solid lines are the characteristics that are measured when the maximum drain bias is 20V. By comparing the low and high voltage curves, a reduction in drain current for $V_{DS} < \sim 6\text{V}$ is noted. This is referred to as current collapse. The fact that it has been observed with GaN MESFETs [2] (as well as HEMTs) and that it is related to buffer layer properties (see below) indicate that this is due to electron trapping in the buffer layer. The downward slope in the drain current for a drain bias > 10 V is attributed to self-heating.

This current collapse phenomenon has a time dependence. After a sufficient time lapse of time, the normal drain current characteristics are restored. The temporal response of the current collapse phenomenon can be investigated through the use of drain lag measurements. Drain lag measurements are also useful for quantifying this effect since devices that exhibit minimal current collapse also exhibit minimal drain lag. Drain lag measurements for several devices are shown in Fig. 7. For these measurements, the device is taken from a low-voltage (10-100 mV) equilibrium condition to a high V_{DS} value (15-20 V) and then returned to the low V_{DS} value. A typical long-term drain lag characteristic is given by curve A in Fig. 7. This device has a drain lag ratio, DLR, (the ratio of I_{DS} values immediately before and after the application of the high drain bias) of 0.85. Significantly lower DLR values have been measured. For device B, the DLR is 1. Devices A and B were fabricated on the same wafer, but the buffer conductivity varied across

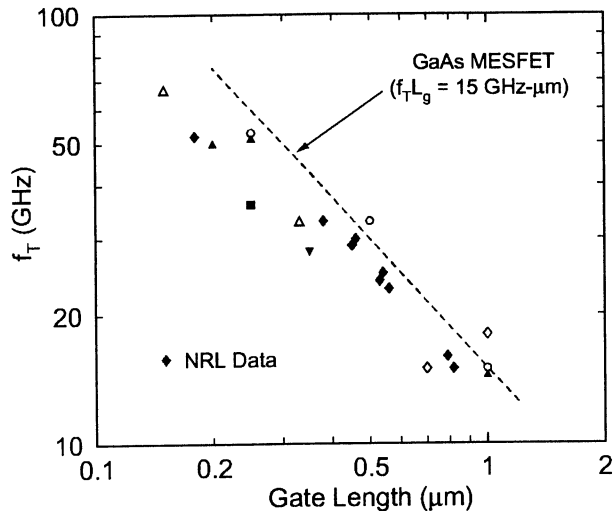


Fig. 5. Cut-off frequency, f_T , as a function of gate length for GaN HEMTs. The different symbols correspond to results from different organizations.

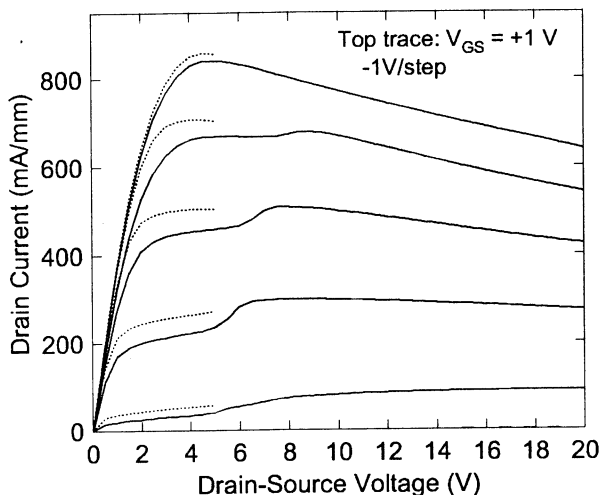


Fig. 6. HEMT drain characteristics. The difference in the low and high bias characteristics is consistent with electron trapping in the buffer layer.

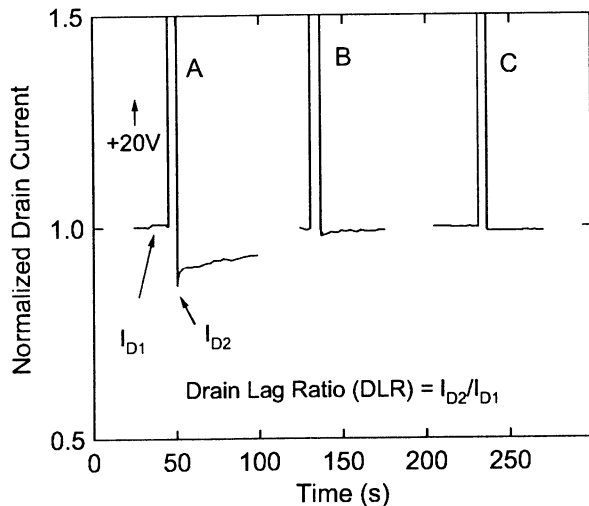


Fig. 7. Drain lag measurements. The drain current normalized to low-field value. A: typical response. B: device on conductive buffer. C: device on a GaN buffer with $10^5 \Omega\text{-cm}$ resistivity.

this wafer. On the conductive parts of the wafer, where the drain current could not be pinched off beyond 15% of I_{\max} , the DLR was 1. The degree of drain lag is apparently related to the conductivity of buffer layer. The deep levels responsible for producing the high resistivity material are also likely to be responsible for this trapping effect. The observed response on conductive buffers is consistent with fewer traps in the conductive buffer regions, or with the filling of these traps by shallow donors. It is possible to produce devices with no drain lag on a resistive ($10^5 \Omega\text{-cm}$) buffer, as is the case for device C in Fig. 7.

DRAIN CURRENT TRANSIENTS: GATE LAG

Gate lag measurements, the drain current response to a gate voltage pulse, have also been made. Shown in Fig. 8 are the two extremes in gate lag response that have been observed. Very limited drain current response, shown by curve B, and nearly complete response, shown by curve A, are indicated. The gate lag phenomenon is usually attributed to surface states in the access regions between the metal contacts that act as electron traps. Although additional study is necessary to establish with certainty that surface states are involved in the observed gate lag phenomena in GaN, the observation that the gate lag response dramatically improves with the addition of a Si_3N_4 dielectric layer is consistent with a surface trapping effect. The degree of gate lag has been previously correlated with microwave output power, in samples that did not have a nitride passivation [3], as shown in Fig. 9. The nitride passivated devices shown here have a similar correlation of gate lag with microwave power output.

MICROWAVE POWER PERFORMANCE

The microwave power performance of GaN HEMTs similar to those described above have been measured. Under CW bias, a power output of 3.1 W/mm with 42% power-added efficiency and 9.7 dB gain was measured at 3.8 GHz. In addition to the trapping effects described above, thermal effects can also limit the power output of GaN HEMTs, especially those grown on sapphire substrates. Pulsed microwave measurements, which utilize a pulsed drain bias, can be used to distinguish between these two effects in that they eliminate a large component of the self-heating.

Pulsed microwave measurements at the same V_{DS} setting of 20 V used for the CW result above resulted in an increase in power density to 4.3 W/mm. The increase in performance under pulsed operation is attributed to a higher drain current level associated with a lower operating temperature in the device active region. Under pulsed conditions it was also possible to bias the devices at higher drain voltages and thus increase the output power in this manner. At a V_{DS} of 35 V, 5.9 W/mm with 37% PAE and 12 dB gain were measured. Comparable performance to this is shown in Fig. 10. These CW and pulsed results are among the highest achieved for

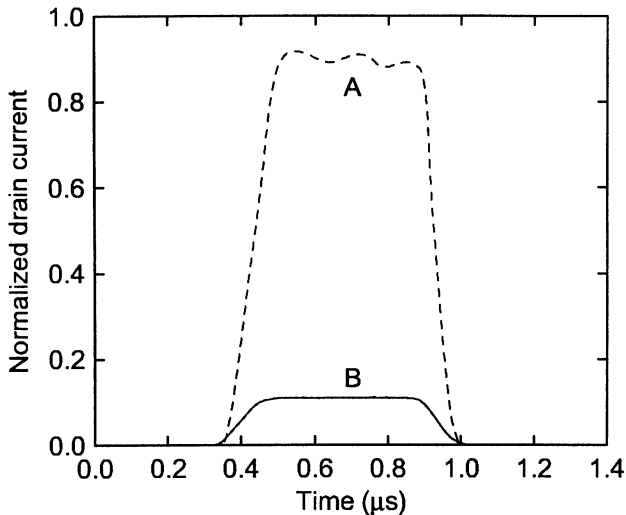


Fig. 8. Gate lag measurement. The drain current is normalized to the equilibrium value of I_{DSS} . A: with Si_3N_4 , B: same device before Si_3N_4 . V_{GS} is pulsed from V_{th} to 0V.

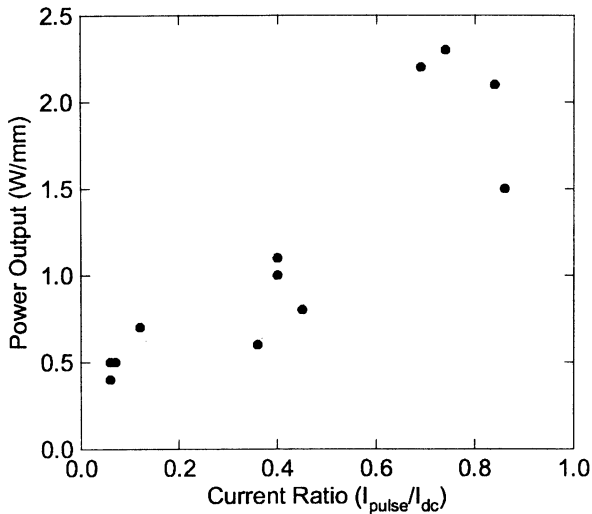


Fig. 9. Correlation of power output with gate lag.

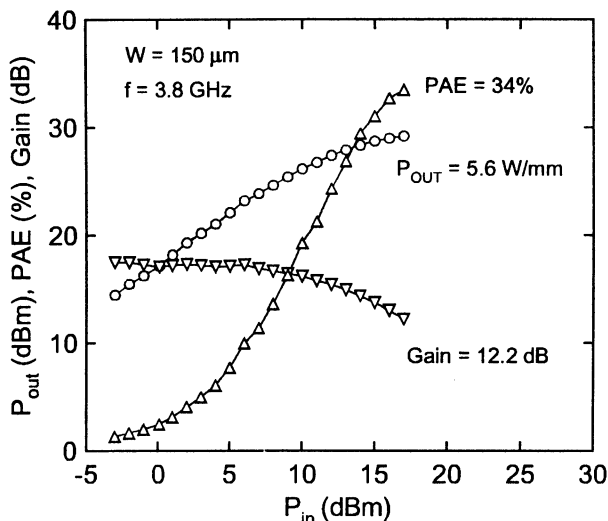


Fig. 10. Pulsed power performance (5 μs pulse width, 1% duty).

GaN HEMTs on sapphire substrates and are significantly higher than what can be achieved with other III-V technologies.

SUMMARY

Excellent high power density results have been demonstrated with the GaN HEMT technology. The present device demonstrations indicate that this will become a viable technology, however, there are a number of issues that need to be resolved to make it manufacturable. Trapping effects in GaN HEMTs need to be eliminated to improve the level of consistency in device performance. Materials and device studies directed toward an understanding and elimination of these trapping effects are currently an active area of research.

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