A Manufacturable Multi-Level Interconnect Process Using Two Layers of 4.5μm-Thick Plated Gold

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ABSTRACT

This paper describes a metal interconnnect process which uses two layers of thick plated gold and thick polyimide intermetal dielectric. The fabrication process is described and results are presented. The results include via yield, initial reliability testing, transmission line characteristics and inductor characteristics.

INTRODUCTION

The addition of a second global level of very thick plated gold interconnect (with very thick interlayer dielectric for low capacitance cross-overs) to our GaAs IC manufacturing process, enables substantial performance improvements and cost reductions of high-efficiency power amplifiers and multifunction MMICs. This Multi-Level Plating (MLP) process allows the fabrication of very low-loss transmission lines[1], very high current bias lines, low-loss spiral inductors, three-dimensional inductors, performance-enhanced couplers and improvements in other useful circuit elements such as divider/combiners and narrow-band filters for high performance MMIC applications. In addition to performance enhancements, the MLP process provides a means for circuit compaction by enabling replacement of distributed matching networks with high-performance lumped elements while simultaneously shrinking the size of these elements. The benefit here is obvious: smaller die size translates directly to lower fabrication cost per IC.

PROCESS DETAILS

The fabrication process used for MLP builds upon our production process for MMICs and RFICs. Table 1 lists the layer names and layer descriptions for the MLP process. The production process, shown in figure 1, features a half-layer of gold interconnect metal (metal 1) deposited and patterned by e-beam evaporation and liftoff. The 0.6 μm thick metal 1 is used in the formation of transistors, resistors, and capacitors. A second layer of interconnect (metal 2) is formed from thick gold plating which is selectively electroplated using a thick photoresist mask. Polyimide is used as the interlevel dielectric (ILD1) and also as the scratch protection or buffer layer for protection of the finished circuitry[2]. The MLP process, shown in figure 2, adds a second layer of thick gold plating (metal 3) and a second layer of polyimide interlayer dielectric (ILD2).

Both plated gold layers are 4.5 μm thick while the first and second polyimide interlayer dielectrics are 3μm and 7 μm thick respectively. All four of these layers are patterned in thick photoresist (6-15 μm) with an I-line stepper. The buffer layer, which uses even thicker photoresist, is exposed on a contact aligner. An oxygen reactive ion etch transfers the resist pattern into the polyimide. The resist thickness must be sufficient to accommodate the topology on the wafer and the erosion during the etch.

The addition of the second layer of gold plating and second layer of thick polyimide interlevel dielectric allows the construction of several types of transmission lines. For example: Both layers of gold plating may be stacked to give a total of 9 μm of gold metal. Gold plating 4.5 μm thick may reside on 0, 3, or 10 μm of polyimide. Two thick gold transmission lines may sandwich 7 μm of polyimide. These various transmission lines are used according to the conductivity, isolation, or coupling needed for a particular application.

RESULTS

Via chains are used to evaluate the MLP interconnect process. One set of via chains consist of metal 1 segments connected to metal 2 segments through vias in ILD1. Each chain contains 48 vias. The resistances of each chain and an equivalent length of metal one and metal two are measured. The metal one and metal two resistances are subtracted from the chain resistance and the result is divided by the number of vias to provide a resistance per via. The via chain yield is the percentage of vias chains with an average via resistances less than 0.3 ohms. Via chain yield versus via size for ILD1 is shown in figure 3. A second set of chains consists of metal 2 segments connected to metal 3 segments through vias in ILD2. The via chain yield versus via size for the 7 micron thick ILD2 polyimide is presented in figure 4.

The first reliability testing done on the new interconnect process was to subject these same via chains to thermal cycling. The via chain yield was measured before and after two hundred thermal cycles from –60C

to 150C. The results of the test are presented in table 2. Only the ILD1 via sizes which had less than 100% yield before the thermal cycling showed degradation from the test.

The thick gold metal 2 and metal 3 conductors are used to form microstrip structures in MMICs. Microstrip lines on GaAs become lossy when GaAs substrates are thinned to 50-75 μm which is necessary for thermal considerations when fabricating high power amplifiers. Adding a polyimide layer beneath the conductor, increases the characteristic impedance of the microstrip line thereby reducing losses. The polyimide dielectric constant (3.2) and loss tangent (0.005) lower the effective dielectric constant for the microstrip line on the thin GaAs substrate.[1] Table 3 shows how the impedance Z_0, the effective dielectric constant ε_{re} and the loss tangent α vary with the polyimide thickness and linewidth. Microstrip lines on 14 μm of polyimide have about half the dissipation loss and about 40% higher characteristic impedance than our standard microstrip lines on GaAs using the same conductor width. The MLP process allows construction of microstrip lines in 4.5 μm of gold plating on 0, 3, or 10 μm of polyimide. An added benefit of the microstrip lines on polyimide is the lines are less capacitive and more inductive which makes them better suited for use in low loss matching networks for active devices.

Improvements in the microstrip line characteristics with the MLP process also led to improvements in the performance of inductors. Our "standard inductor" is fabricated with the metal two coil on the GaAs substrate and a metal one connection from the coil center to the output with ILD1 in the crossover between metal one and metal two. Our "multi-level inductor" is fabricated with the coil in metal three on ten microns of polyimide and a metal 2 connection to the coil center through a via in ILD2. The third inductor design is the "3D inductor". The 3D inductor has a coil in metal three on ten microns of polyimide and another coil in metal two on three microns of polyimide. The upper and lower coils are connected through a via in ILD2. Table 4 shows some measured results which reveals the performance differences for these three construction techniques.[3,4] The 6.7 nH inductor measurements show the multi-level inductor has 28% higher resonant frequency (f_{res}) and 50% higher quality factor (Q) than the standard inductor. The improvements are due to the reduced resistance of the multi-level inductor which uses 4.5 μm thick gold plating exclusively compared to the 0.6 μm evaporated metal one layer and the 4.5 μm metal two used together in the standard inductors. Additional improvement is due to the thick polyimide layers of the multi-level inductor providing reduced dissipated loss and lower parasitic capacitance. The 6.7 nH 3-D inductor compared to the standard inductor showed an 11% decrease in f_{res}, a 29% increase in Q, and a 56% decrease in area. The 3-D inductor uses the muti-level interconnect process so it also benefits from the reduced resistance of the metal two and metal three conductors and improved isolation from the substrate with the polyimide. The stacked coils provide a much higher inductance per unit area but the increased capacitance between the coils reduces the f_{res}. One last attribute to note is the current capacity of the inductors. The inductors constructed from metal 2 and metal 3 are capable of handling 13.5 mA/μm of conductor width based on a maximum current density of $3X10^5$ A/cm^2. Consequently 10, 20, and 40 μm conductor widths may carry 135, 270 and 540 mA respectively.

The MLP processes allows compaction of the IC mostly by means of converting distributed matching to lumped-element matching. The use of lumped elements is possible due to the improved performance of the passive components. We achieved a 50% size reduction in a high-efficiency X-band 10 W power amplifier using the MLP process.

CONCLUSIONS

In conclusion, we have developed a manufacturable, thick-plating, multi-level interconnect process which enables IC performance improvements and chip-size reduction . The transmission lines and inductors were improved by the insulating properties of the polyimide and the reduced resistance of the plated gold. Using the improved passive elements available with the MPL process, we lowered cost for a 10 W X-band power amplifier by reducing the chip size 50%.

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Buffer Layer	7 µm of polyimide
Metal 3	4.5 µm of plated gold
ILD2	7 µm of polyimide
Metal 2	4.5 µm of plated gold
ILD1	3 µm of polyimide
Metal 1	0.5 µm of evaporated gold

Table 1. Process Layers

ILD #	Via Size (µm)	0 cycle yield (%)	200 cycle yield (%)	Change (%)
1	3.5	68	6	62
1	4.0	76	53	23
1	4.5	100	100	0
1	5.0	100	100	0
1	5.5	100	100	0
1	6.0	100	100	0
1	6.5	100	100	0
2	4.5	99.5	99.5	0
2	5.0	100	100	0
2	5.5	100	100	0
2	6.5	100	100	0
2	7.5	100	100	0
2	8.5	99.5	99.5	0
2	10.5	99.5	99.5	0

Table 2. Yield before and after thermal cycles.

Polyimide Thickness (µm)	Microstrip Width (µm)	Measured Z_0 (Ω)	Measured ε_{re}	α(dB/cm) @ 20 GHz
0	20	69.0	7.65	1.07
0	50	50.0	8.23	0.83
0	100	35.8	8.90	0.70
0	150	32.0	9.40	0.61
3	20	81.0	5.30	0.85
3	50	57.0	6.40	0.68
3	100	41.0	7.00	0.55
3	150	32.0	7.60	0.48
7	20	92.0	4.35	0.69
7	50	64.1	5.25	0.50
7	100	45.0	6.00	0.41
7	150	35.5	6.55	0.37
14	20	105.0	3.70	0.55
14	50	75.0	4.30	0.40
14	100	53.0	5.00	0.35
14	150	42.0	5.40	0.30

Table 3. Microstrip characteristics for 75 µm GaAs substrate

Inductance	Type	Current Capacity	f_{res}	Q at ½ f_{res}	Area
(nH)		(mA)	GHz		mm^2
6.7	Standard	72	5	22.0	0.193
6.7	Multilayer	270	6.4	33.0	0.193
6.7	3-D	270	4.43	28.5	0.084
1	Standard	72	20.85	29.0	0.055
1	Multilayer	270	24.6	43.8	0.055
0.5	3-D	1080	20	30.5	
0.284	3-D	540	40	33	

Table 4. Inductor characteristics for 75 µm GaAs substrate

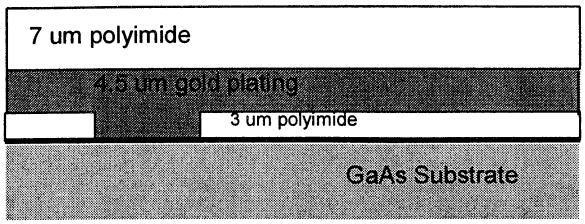

Figure 1. Interconnnect for production process

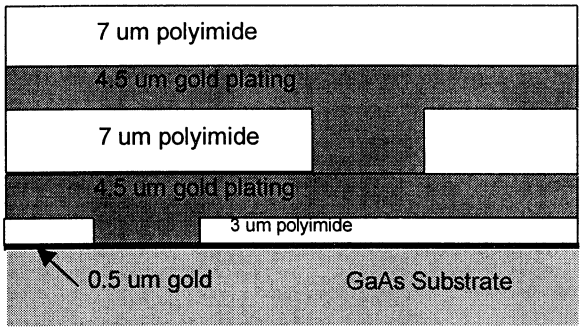

Figure 2. Interconnect for MLP process

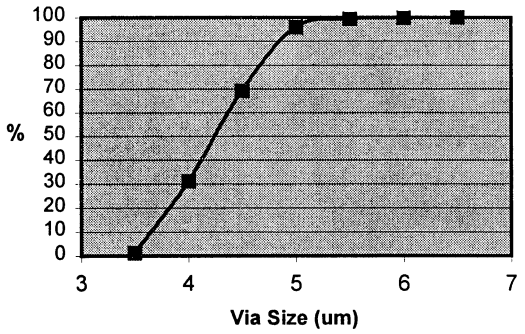

Figure 3. ILD1 via chain yield

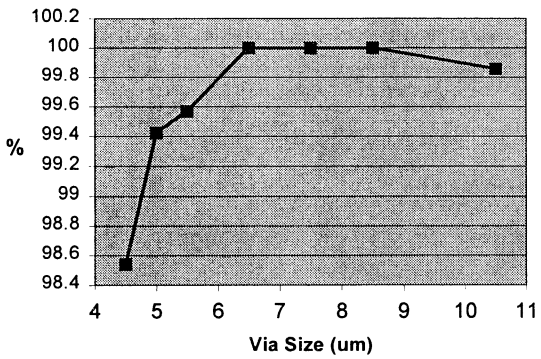

Figure 4. ILD2 via chain yield