0.1 μm InGaAs/AlGaAs/GaAs HEMT MMIC Production Process for High Performance Commercial Ka-band LNAs

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ABSTRACT

We present a 0.1 μm InGaAs/AlGaAs/GaAs HEMT (GaAs HEMT) MMIC process for high volume, low cost Ka-band low noise amplifier applications. This process has achieved both state-of-art MMIC low noise performance including 1.3 dB noise figure at 30 GHz and 2.0 dB noise figure at 38 GHz (both with greater than 20 dB associated gain), high r.f. yield in excess of 80% and superb reliability with a high activation energy of 1.7 eV and a mean time to failure of 6 billion hours (~60,000 years) at a channel temperature of 125C.

INTRODUCTION

Current and future commercial LMDS and satellite transceiver modules require low cost and high performance millimeter-wave MMICs at Ka-band. A lower noise figure MMIC receiver amplifier is desired to a) reduce the required transmitter power which is one of the most costly components in the transceiver, b) provide performance margin that allows for less MMIC screening and increases overall yield and c) leverage MMIC-based approach to eliminate bonding and tuning.

PROCESS AND MMIC DESCRIPTION

To provide low noise figure at Ka-band for a GaAs HEMT process, we have developed a highly reproducible, high yield 0.1 μm T-gate InGaAs/AlGaAs/GaAs HEMT device and MMIC process[1]. The device profile shown in Figure 1 is designed to minimize short channel effects and ensure good device pinchoff and adequate gate-drain breakdown greater than 6V. The pseudomorphic AlGaAs/InGaAs/GaAs HEMT profile also ensures high maximum current density. A 0.1 μm HEMT device with this profile demonstrates transconductances greater than 600 mS/mm, cutoff frequencies greater than 120 GHz at 2V drain bias and maximum oscillation frequencies greater than 200 GHz. The process includes a thin 750Å PECVD silicon nitride passivation to minimize feedback capacitance and other parasitic capacitances.

We have achieved excellent wafer to wafer device parameter repeatability on over a hundred recently fabricated 0.1 um GaAs HEMT wafers, including very tight gate length control (Lg = 0.10 +/- 0.01 μm), measured on every wafer with SEM. Vp control is also very tight with a typical standard deviation of 80 mV wafer to wafer. Excellent results have been achieved on the best LNA MMIC chips, exceeding previous results fabricated using R&D processes. A 2-stage single ended 30 GHz low noise amplifier demonstrated as low as 1.2 dB noise figure with 25 dB associated gain (data shown in Figure 2). The design employs a single supply voltage with an on-chip source resistance feedback to self-bias the transistors to a nominal current of 70 mA. Another 2-stage single-ended on-chip self biased 38 GHz low noise amplifier, demonstrated as low as 2.0 dB noise figure with 20 dB associated gain (data shown in Figure 3). Based on statistical simulation, the noise figure cumulative yield distribution for the 38 GHz LNA design shows wafer average noise figures between 2.1 to 2.5 dB at 38.5 GHz as shown in Figure 4. The tight distribution is due to the excellent Lg and Vp control of the process. The drain current standard deviation based on the expected device distribution is less than 5% wafer to wafer. To our design specification of 3.0 dB, MMIC yield greater than 85% has been achieved on this process, with almost all of the yield loss occurring due to lack of circuit functionality. The extremely high yield allows less r.f. screening and chip tuning which reduces overall chip cost.

RELIABILITY

We have conducted a full 3-temperature accelerated lifetest on 2-stage 44 GHz LNA MMIC samples on the 0.1 μm GaAs HEMT process. The lifetest was conducted in ambient air. At each temperature as many as 30 LNA samples were lifetested. An initial 48 hour burn-in at 150C was conducted on all the samples. Channel temperatures of 330C, 315C and 300C were selected for the 3-temperature lifetest. A drain bias voltage of 4.2V with a constant current bias of 36 mA (150 mA/mm) was applied to the MMICs. A temperature rise of 45C was assumed based on thermal simulation of the device and MMIC chip design. The failure criteria was 1.0 dB degradation in r.f. gain measured in predetermined time intervals. 1.0 dB gain degradation is correlated with less than 0.5 dB noise figure degradation for these LNAs. The mean time to failures were 158 hours at 330C, 496 hours at 315C, and 923 hours at 300C. The calculated activation energy is 1.7 eV with a mean time to failure extrapolated back to 125C channel temperature of 6 billion hours or equivalently 60,000 years as shown in Figure 5. These results exhibit the excellent reliability of the 0.1 μm GaAs HEMT process.

These results demonstrate our unique capability to produce large quantities of high performance Ka-band LNA HEMT MMIC chips with extremely high yield and reliability which will lead to lower cost and high throughput MMIC-based transceivers for LMDS and commercial satellite applications.

[1] R. Lai et. al., "A 0.15 mm InGaAs/AlGaAs GaAs HEMT Production Process for High Performance and High Yield V-band Power MMICs", 1995 IEEE GaAs IC Symposium Tech. Digest, p. 105

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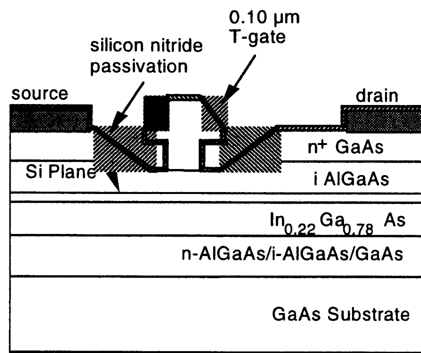

Figure 1. Device cross section for 0.1 μm InGaAs/AlGaAs/GaAs HEMT

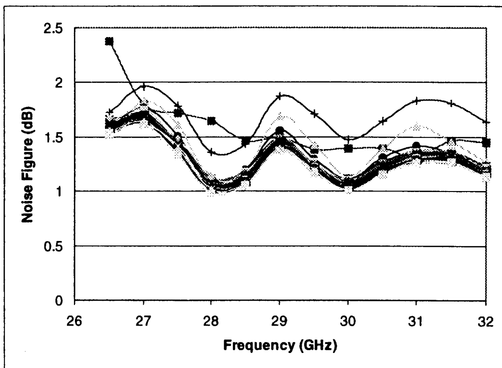

Figure 2. Noise figure performance for 30 GHz LNA
Vd = 5V, Id = 60 mA nominal; Gain ~25 dB

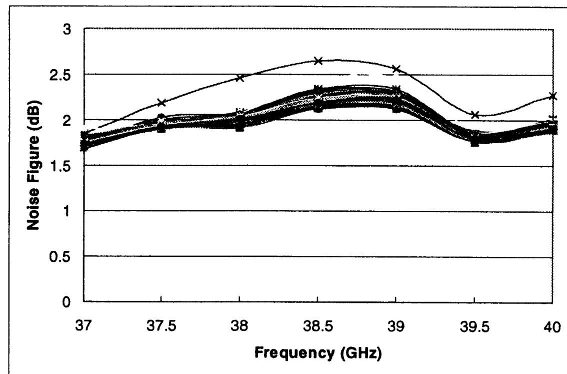

Figure 3. Noise figure performance for 38 GHz LNA
Vd = 5 V, Id = 60 mA nominal; Gain ~20 dB

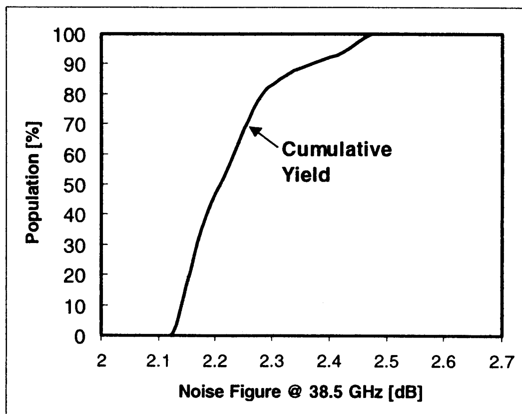

Figure 4. Statistical simulation of wafer average noise figure at 38.5 GHz

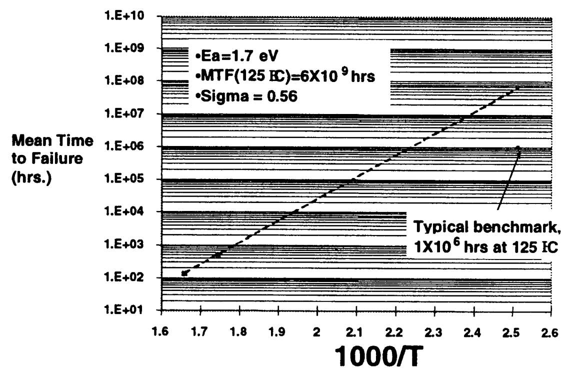

Figure 5. Arrhenius plot of mean time to failures for 3 temperature lifetest on 0.1 um GaAs HEMT MMIC LNA. Failure at δS21 > 1.0 dB. Lifetest was conducted at Vd = 4.2V & Id = 36 mA (150 mA/mm)

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