

## Challenges in Rapidly Scaling up Back-side Processing of GaAs Wafers

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### ABSTRACT

The dramatic increase in demand for GaAs based pHEMT and HBT devices has required the expansion of wafer FAB capacity. One of the major challenges in expanding FAB capacity lies in the back-side process area. Historically, most GaAs back-side wafer process steps had been very labor intensive since there was not much available in manufacturing equipment to support these steps. Yield had often depended on the skill of experienced technicians. A number of back-side process steps have recently been changed and/or automated in order to dramatically increase throughput and improve yield. GaAs FAB process engineers are working closely with equipment vendors to further optimize and qualify new equipment for the back-side area.

### INTRODUCTION

A description of the various steps involved in back-side processing for GaAs wafers is given below. Figure 1 shows a cross-sectional view of the major steps as the GaAs wafer undergoes backside processing with via-holes.<sup>1</sup> The following steps are performed after completion of final front-side DC electrical test.

1. For back-side via-hole processing, the wafers are mounted onto flat carriers with the front-sides adjacent to a thermoplastic mounting medium or high temperature wax.<sup>2-5</sup> The most widely used flat carriers are fabricated from sapphire, which is thermally compatible with GaAs, resistant to most wet chemical etch solutions, and can be machined to an optically flat surface. For GaAs devices that do not require backside vias or front-side airbridges, back-grinding (BG) tape<sup>6</sup> or a thick photoresist layer can be applied to protect the wafer front-sides during thinning operations.
2. The wafers are thinned to the desired thickness range by using a combination of the following techniques: grinding<sup>5-10</sup>, lapping<sup>1, 11</sup>, polishing<sup>11</sup>, and/or wet immersion<sup>5, 12, 13</sup> or spray etching<sup>6, 10</sup>. For high volume applications rough grinding is usually employed followed by polishing, spray etching, or an immersion etch to remove several μms of residual grinding damage.<sup>5, 10</sup> Rough grinding followed by slower speed fine grinding and immersion or spray etch to remove a few μms of residual damage is also used.<sup>1, 6-9</sup>
3. For GaAs wafers that do not require back-side vias or front-side airbridges, the back-grinding (BG) tape can be

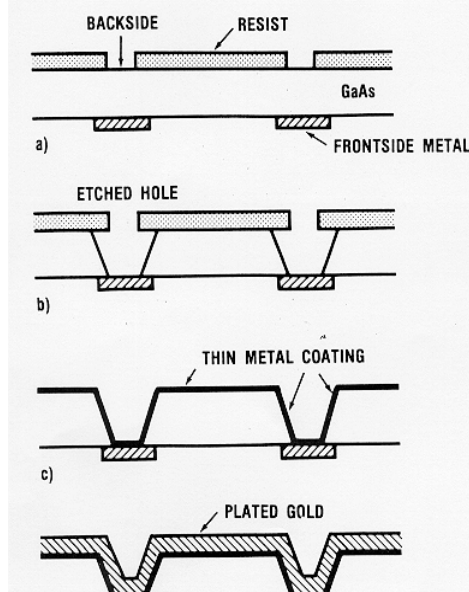


Fig. 1: Backside via processing steps.<sup>1</sup>

removed with a wafer de-taping system<sup>6</sup> or the protect photoresist can be wet stripped. For GaAs wafers thinned using BG tape, ultra-violet (UV) sensitive tape is utilized since the UV exposure before peeling reduces the tape adhesion strength by at least an order of magnitude. UV BG is extensively used for very thin silicon wafer Smart card applications.<sup>6</sup> Most automatic wafer de-taping systems offer a UV exposure module option. The UV BG de-tape step can be done after the dice tape frame mount step, so that the thinned wafer is continuously supported with tape from the grind through dice steps. Wafer tape system vendors are developing new cassette to cassette tools that combine these two steps.<sup>14</sup> The process flow for non-via devices continues at step 8 below. For via-hole processing, the via mask is defined on the backside wafer surfaces using a thick photoresist layer and either an infrared (IR) contact or dual-side image mask aligner.<sup>1</sup> After the photoresist masks are hardened with a post-bake, the via holes are etched using either reactive ion etch (RIE)<sup>15-23</sup> or inductively coupled plasma (ICP)<sup>24-26</sup>. Batch RIE systems, which can handle up to four 100 mm diameter wafers per run, have been widely used. However, single wafer ICP is being employed as GaAs FABs convert to processing 150 mm diameter wafers.<sup>26</sup>

4. The thick photoresist mask is stripped from the back-side wafer surfaces with a stripper solution followed by exposure to a high oxygen content plasma environment.<sup>1</sup> Depending

on the aggressiveness of the photoresist cross-linking and the via hole etch conditions, the stripper solution may need to be either sprayed onto the wafer backside surfaces or the wafers need to be immersed and agitated in heated stripper solution. However, the immersion technique can result in some leaching of the exposed mounting medium at the thinned wafer / carrier sandwich perimeter. If a wet spray strip technique cannot be utilized, then a high oxygen content RIE can be used to totally remove the residual organics from the backside wafer surfaces prior to seed layer deposition.

5. A seed layer for electroplating is deposited on the backside wafer surfaces by either sputter deposition<sup>1, 16, 18, 27-29</sup>, evaporation<sup>30</sup>, or electroless plating<sup>1, 20, 31, 32</sup>. For sputter deposition either a thin Ti, TiW, or Cr layer is deposited for adhesion between the GaAs and the thin Au conducting layer. For electroless plating either Pd/Au<sup>20, 31-34</sup> or Pd/Ni<sup>34</sup> is used where Pd acts as a catalyst for the subsequent electroless plating of Au or Ni. A thick electroplated Au layer is then deposited onto the seed layer.<sup>1, 18, 27, 31</sup> The electroplated Au must be thick enough to meet thermal conductivity requirements and improve the mechanical strength of the thinned wafer.<sup>31</sup> If a Au-Sn eutectic solder die attach process is subsequently used, then the layer must be thick enough to accommodate leaching of some gold during eutectic solder die attach, so that voiding can be minimized.<sup>1, 30</sup> A batch or cluster sputter deposition tool for the seed layer is amenable to high volume manufacturing and therefore is widely used by most GaAs FABs. Even though the equipment costs for electroless plating are relatively inexpensive, this process step can be difficult to automate for high volume GaAs wafer manufacturing since electroless baths are typically very sensitive to temperature, pH, specific gravity, organic contamination, etc. Some baths are susceptible to spontaneous "plate out".<sup>34</sup> Well trained operators with plating experience would be needed to run a high yielding volume operation. Evaporation is a highly directional deposition process and is therefore not amenable to small, high aspect ratio via holes. If the die are to be attached to ceramic packages using Au-Sn eutectic solder, then a solder "stop" metal layer, such as Ti, Ni, or Cr, that readily oxidizes needs to be deposited inside the vias to prevent solder from "wicking up" and "blowing out" the front-side metal pads.<sup>32</sup> If the die are to be attached using a conductive epoxy, then a solder "stop" layer is unnecessary. A photolithography / wet or dry etch process is typically used to completely clear the solder "stop" metal layer from the back-side metal plane in order to minimize voiding at this interface during the eutectic solder die attach step.

6. If the wafers are to be diced by scribing, then back-side streets may need to be defined by using a photolithography / wet etch process.<sup>1, 36</sup> If the wafers are to be diced by sawing, then streets can be implemented in order to reduce yield loss from sawing through the soft gold layer.<sup>8, 36</sup> It is possible to combine the photolithography steps for solder "stop" and streets by using one contact mask alignment for streets and a

flood exposure followed by a develop step to clear the thick positive photoresist layer from the back-metal surface.

7. If a second back-side photoresist mask is utilized, then it needs to be removed with a stripper solution before the wafer is dismantled from the flat carrier. The thinned wafers can be dismantled from perforated carriers using a heated solvent bath or vapor degreaser system with custom fixturing.<sup>2, 4, 5, 37</sup> During this process step the mounting medium is also removed from the wafers and carriers. The other option for non-perforated carriers is to have skilled operators use a vacuum hotplate and a high temperature vacuum wand tip to slide the carrier from the wafer or vice versa after the mounting medium exceeds its liquid flow temperature.<sup>1, 2, 4, 37</sup> However, the latter method may not be amenable to high volume manufacturing since yield loss tends to be high due to breakage and possible air bridge damage.<sup>2, 4, 37</sup> If the vacuum hotplate technique is used, the dismantled thinned wafers and the carriers are then cleaned in solvent baths to remove the mounting medium. Finally, the thinned wafers are exposed to an oxygen rich plasma environment before inspection and possibly on-wafer RF test.

8. At both inspect and RF test, computer maps are generated to distinguish acceptable die from poor visual and/or electrical die. These maps are fed into and combined in an automatic die pick and place system.<sup>1, 38</sup> For very high yielding devices, electrical test may not be required. After the thinned wafers are mounted onto dicing tape, they are either scribed or sawn.<sup>1, 37</sup> Scribing is preferred since throughput is higher and die street dimensions can be made smaller allowing for more die per wafer. An automatic die pick and place system uses the maps to pick & place the acceptable die into Gel-packs.

9. The die from Gel-packs are attached to packages using an automatic pick & place die bonding system. Depending on the device thermal conduction requirements, automated die bonding systems can be set up to accommodate either the Au-Sn eutectic solder<sup>1, 27-29, 39-43</sup> or the conductive thermoset epoxy.<sup>1, 36</sup> die attach method.

## DISCUSSION

Of the nine backside wafer process steps described above, equipment able to handle high volume 150 mm GaAs wafer manufacturing can currently be purchased and qualified to perform most of these steps. A list of the back-side wafer new process equipment with estimated costs needed to handle a throughput of about 1000 wafers per week for both via and non-via devices is given in Table 1. The total estimated cost is about \$7.2 M. The total estimated equipment cost can be lowered by purchasing used vs. new equipment, specifying batch vs. cluster platforms, and/or foregoing automatic handling where feasible.

Automatic single wafer rough and fine spindle grinding systems originally designed for thinning silicon wafers in Smart card applications<sup>6</sup> have recently been adapted by vendors to handle GaAs wafer thinning. Some of these

systems even offer a spray etch module option for post-grind damage removal. Vendors are also adapting the automatic wafer BG taper and de-taper systems, originally targeted to the very thin silicon wafer (80 to 100  $\mu\text{m}$ ) market, to handle 150 mm GaAs wafers thinned down to as low as 150  $\mu\text{m}$ . Most photolithography equipment vendors can adapt the automatic wafer handlers on coat, bake, and develop tracks to also handle 100 to 50  $\mu\text{m}$  thinned wafers mounted on sapphire carriers. The carriers usually have a diameter between 3 and 9 mm greater than the wafer diameter to eliminate mechanical damage due to misalignment at the mounting step.<sup>3, 5</sup> Back-side IR contact and dual-side image aligners have been steadily adapted over the years to handle the increasing wafer volumes at GaAs and other FABs.

For 150 mm GaAs via etching, several vendors are offering multi-chamber cluster tool configurations. Thus far the chamber of choice has been ICP although dual frequency high density plasma (HDP) reactors have achieved comparable etch rates.<sup>26</sup> For sputter deposition and depending on throughput requirements, it may be possible to perform back-side seed and front-side resistor layer deposition in the same cluster or batch tool. If both layer depositions are to be done in the same tool, the automatic wafer handler must be able to handle both standard and thinned wafers on carriers. Batch systems with automatic wafer handlers originally targeted for silicon wafer flip chip applications are now being adapted to handle both GaAs front-side and back-side wafer processing. However if bias, long throw, or collimated sputter deposition is required to ensure conformal seed layer coverage of high aspect ratio individual source via hole sidewalls, then a cluster platform with individually configured chambers may be required.<sup>44</sup>

Wafer electroplating equipment technology has progressed rapidly over the past few years as a result of copper interconnect metallization for silicon wafers, wafer flip chip and solder bumps, MEMs, etc. However, the higher-end tools targeted for silicon industry may be too costly for most GaAs FABs unless it can be justified by high wafer throughput using Cost of Ownership modeling (CoO). Fortunately, there are several wafer plating vendors, who are targeting the GaAs FAB and optoelectronic markets, with moderately priced tools in the \$300 to \$600K range that can handle up to 1000 wafers per week.

There are still a few key back-side process steps for which equipment needs to be further optimized and automated where possible. Also, these tools have to be made robust and affordable. The key steps include GaAs wafer mounting onto sapphire carrier substrates, mounting adhesive application, and wafer de-mounting from the carrier. For many years vendors have offered inexpensive single wafer / carrier manual vacuum mounting systems for low volume applications that are equipped with a heater and pressure plate or rugged polymer bladder. A few vendors have recently introduced adhesive dispense and mounting modules based on a microlithography cluster platform with automatic handling. In addition to the GaAs market, these new tools

are targeted for the flat panel display industry. The high cost of these new tools will need to be justified by high enough wafer volumes using CoO. Some GaAs FABs are using custom built manual multi-wafer vacuum mounting systems with individual spring loaded pressure plates that can handle up to 1000 wafers per week. These systems are relatively inexpensive but require operators to manually load the individual wafers and carriers and unload the "sandwiches".

Table 1: Major new wafer back-side equipment and estimated costs to handle 150 mm GaAs wafer processing from front-side electrical test to dicing.

Description	\$K	Comments
Automatic wafer taper	135	UV BG tape
Sapphire carriers	765	Perforated
Adhesive coat & bake track	225	High viscosity dispense cartridge
Wafer / carrier mounter	150	Manual multi w/ repeatable centering
Automatic wafer grinder	650	Rough & fine single wafer spindles
Post-grind spray etcher	400	May be combined w/ grinder
Wafer de-taper with UV	140	Handling of thinned wafers
PR coat & bake track	200	Sapphire carrier compatible
Back-side aligner	600	IR or dual-side image
Phororesist develop hood	50	Manual, no robotic handling
Photoresist strip hood	80	Manual, w/ fire suppression
Heated nitrogen dryer (2)	60	For thinned wafers & wafer / carriers
Barrel asher for descum	90	For post develop & dry cleans
Via etch system	1800	Cluster w/ 3 chambers
Sputter deposition system	1200	Batch with auto handling
Wafer electroplater	400	Manual cup or batch
Wet bench for street etch	80	Au & Ti manual batch etch
Wafer / carrier de-mounter	180	Vapor degreaser – perforated carriers
Total	7205	

Most GaAs FABs are now utilizing thermoplastic based mounting adhesives commonly used for packaging and temporary attach applications (see Table 2). Thermoplastic adhesives can be diluted in a solvent and applied as a liquid using a high viscosity pump or cartridge dispenser added to a standard photoresist coat & bake track. However, residual adhesive can dry out and clog the dispense tip after dispense. FAB process engineers need to work carefully with photoresist track and high viscosity dispense system vendors to find a robust, reliable, and affordable dispense method.

Thermoplastic adhesives can also be applied as a dry film using a vacuum bladder or heated roller laminator both widely used by the printed circuit board industry for negative dry film photoresist application. However if dry film roller lamination is used on wafers, precautions must be taken to ensure that air bridges are not crushed during lamination. The vacuum bladder laminator tends to be more forgiving and can be optimized to minimize trapped air voids in between the dry film and wafer front-side surface topography. If a dry film thermoplastic adhesive is used, then the sapphire carriers must be perforated to allow for wafer de-mounting in either a vapor degreasing system<sup>5</sup> or a solvent bath. The viscosity of room temperature dry film thermoplastics that are heated above the bonding temperature ( $T_b$ ) are usually too high to utilize a de-mount method based on vacuum clamping the heated wafer and carrier and sliding

the wafer and carrier apart. Note that perforated carriers cost about \$500 more per carrier than non-perforated.

Table 2: Thermoplastic based and other adhesives used by GaAs FABs.

Trade Name	Manufacturer	Dry or Solvent	T <sub>b</sub> (°C)
WF5801	Ablestik	Dry film	140
Staystik 432	Alpha Mtls-Cookson	Dry film	150
Staystik 336T	Alpha Mtls-Cookson	Petroleum Ether	125
Crystalbond 509	Aremco	Acetone or GenSolve™	120
Pentalyn-H <sup>5</sup>	Hercules	Xylene	110

Currently, there are vendors experimenting with the vacuum clamping heat / slider method for de-mounting 150 mm wafers mounted on non-perforated carriers attached using a liquid dispensed thermoplastic. The biggest challenge in developing a robust, automated system is handling the thinned wafer after slider de-mount. This may require the use of a contactless thin wafer handler based on the Bernoulli principle.<sup>6</sup>

#### SUMMARY

The process steps involved in back-side GaAs wafer processing were reviewed for devices requiring vias and metallization and non-via devices. Equipment and process issues involved in scaling up manufacturing to handle high volume 150 mm GaAs wafers were presented.

#### REFERENCES

<sup>1</sup>R. Williams, Modern GaAs Processing Techniques, Artech House, Inc., Norwood, MA, 1990.  
<sup>2</sup>K. M. Adams and L. S. Klingbeil, *GaAs MANTECH Conf. 2000*, p. 75-78.  
<sup>3</sup>M. P. Norman and W. R. Griffith, *GaAs MANTECH Conf. 1992*, p. 19-21.  
<sup>4</sup>A. Quach, J. Smith, A. Stark, N. Wylie, K. Stanley, and D. Thayer, *GaAs MANTECH Conf. 1994*, p. 69-72.  
<sup>5</sup>J. Crites, *GaAs MANTECH Conf. 1995*, p. 44-46.  
<sup>6</sup>J. Muller, P. Stamka, W. Kroninger, E. Gaulhofer, and H. Oyrer, *Semicond. Internat.* **23**(7), 191 (2000).  
<sup>7</sup>M. Nishiguchi, N. Goto, T. Sekiguchi, H. Nishizawa, H. Hayashi, and K. Ono, *IEEE Trans. Comp., Hybrids, and Manuf. Technol.* **13**, 528 (1990).  
<sup>8</sup>M. Nishiguchi, A. Miki, N. Goto, M. Fujihira, H. Nishizawa, H. Hayashi, and K. Ono, *IEEE Trans. Comp., Hybrids, and Manuf. Technol.* **14**, 848 (1991).  
<sup>9</sup>M. Nishiguchi, N. Goto, and H. Nishizawa, *IEEE/CHMT IEMT Symp. 1993*, p. 1072-1080.  
<sup>10</sup>M. E. Grupen-Shermansky and C. L. Pilote, *GaAs MANTECH Conf. 1994*, p. 167-170.  
<sup>11</sup>K. W. Torrance, J. McAnemy, and M. Robertson, *GaAs MANTECH Conf. 1999*, p. 183-185.  
<sup>12</sup>J. M. O' Connor, E. F. Dvorsky, H. S. Hier, and W. F. Reif, *J. Electrochem. Soc.* **135**, 190 (1988).  
<sup>13</sup>K. Bock, A. Grub, and H. L. Hartnagel, *J. Electrochem. Soc.* **137**, 3301 (1990).  
<sup>14</sup>For example: Nitto Denko America, Inc., Model MHR-8500 wafer dice tape mounter, Fremont, CA.  
<sup>15</sup>K. Sumitani, M. Komaru, M. Kobiki, Y. Higaki, Y. Mitsui, H. Takano, and K. Nishitani, *GaAs IC Symp. Tech. Dig. 1989*, p. 207-210.  
<sup>16</sup>T. Nguyen and T. White, *GaAs MANTECH Conf. 1992*, p. 23-26.  
<sup>17</sup>K. J. Nordheden, D. W. Ferguson, and P. M. Smith, *J. Vac. Sci Technol. B* **11**, 1879 (1993).  
<sup>18</sup>M. L. Lovejoy, R. J. Shul, C. Constantine, and D. J. Rieger, *GaAs MANTECH Conf. 1994*, p.171-174.  
<sup>19</sup>Camacho and D. V. Morgan, *J. Vac. Sci Technol. B* **12**, 2933 (1994).

<sup>20</sup>S. J. Pearton, F. Ren, C. R. Abernathy, and C. Constantine, *Mat. Sci. and Eng.* **B23**, 36 (1994).  
<sup>21</sup>R. J. Shul, M. J. Lovejoy, J. C. Wood, A. J. Howard, D. J. Rieger, and S. H. Kravitz, *J. Vac. Sci Technol. B* **15**, 657 (1997).  
<sup>22</sup>K. J. Nordheden, X. D. Hua, Y. S. Lee, L. W. Yang, D. C. Streit, and H. C. Chen, *J. Vac. Sci Technol. B* **17**, 138 (1999).  
<sup>23</sup>J. Lee, H. Tsai, Y. S. Chang, and R. T. Huang, *GaAs MANTECH Conf. 2000*, p. 71-74.  
<sup>24</sup>R. J. Shul, G. B. McClellan, R. D. Briggs, D. J. Rieger, S. J. Pearton, C. R. Abernathy, J. W. Lee, C. Constantine, and C. Barratt, *J. Vac Sci Technol. A* **15**, 633 (1997).  
<sup>25</sup>E. W. Berg and S.W. Pang, *J. Electrochem. Soc.* **146**, 775 (1999).  
<sup>26</sup>R. Szweda, *III-Vs Review* **13**(5), 48 (2000).  
<sup>27</sup>T. Ishikawa, K. Okaniwa, M. Komaru, K. Kosaki, and Y. Mitsui, *IEEE Trans. Elec. Dev.* **41**, 3 (1994).  
<sup>28</sup>C. C. Lee and G. S. Matijasevic, *IEEE Trans. Comp., Hybrids, and Manuf. Technol.* **12**, 406 (1989).  
<sup>29</sup>M. Nishiguchi, N. Goto, and H. Nishizawa, *IEEE Trans. Comp., Hybrids, and Manuf. Technol.* **14**, 523 (1991).  
<sup>30</sup>G. Hampton and D. M. Jacobson, *Gold Bull.* **22**(3), 79 (1989).  
<sup>31</sup>L. A. D'Asaro, J. V. DiLorenzo, H. Fukui, *IEEE Trans. Elec. Dev.* **ED-25**, 1218 (1978).  
<sup>32</sup>L. A. D'Asaro, S. Nakahara, and Y. Okinaka, *J. Electrochem. Soc.* **127**, 1935 (1980).  
<sup>33</sup>D. Lamouche, P. Clechet, and J. R. Martin, *J. Electrochem. Soc.* **130**, 2255 (1983).  
<sup>34</sup>G. O. Mallory and J. B. Hajdu (ed.), Electroless Plating: Fundamentals and Applications, American Electroplaters and Surface Finishers Society, Orlando, FLA, 1990.  
<sup>35</sup>L. G. Svendsen, T. Osaka, I. Koiwa, and H. Sawai, *J. Electrochem. Soc.* **130**, 2255 (1983).  
<sup>36</sup>D. L. Monthei, Package Electrical Modeling, Thermal Modeling, and Processing for GaAs Wireless Applications, Kluwer Academic Publishers, Norwell, MA, 1999.  
<sup>37</sup>W. C. Howell, *GaAs MANTECH Conf. 1990*, p. 48-51.  
<sup>38</sup>H. Ignatius, D. Huntley, *Solid State Technol.* **42**(6), 119 (1999).  
<sup>39</sup>J. S. Pavo, *IEEE Trans. Electron Devices* **ED-34**, 2616 (1987).  
<sup>40</sup>G. S. Matijasevic and C. C. Lee, *J. Electron. Mat.* **18**, 327 (1989).  
<sup>41</sup>C. C. Lee and G. S. Matijasevic, *IEEE Trans. Comp., Hybrids, and Manuf. Technol.* **12**, 406 (1989).  
<sup>42</sup>C. C. Lee, C. Y. Wang, and G. S. Matijasevic, *IEEE Trans. Comp., Hybrids, and Manuf. Technol.* **14**, 407 (1991).  
<sup>43</sup>M. Nishiguchi, N. Goto, and H. Nishizawa, *IEEE Trans. Comp., Hybrids, and Manuf. Technol.* **14**, 523 (1991).  
<sup>44</sup>R. A. Powell and S. M. Rossnagel, Thin Films PVD for Microelectronics: Sputter Deposition Applied to Semiconductor Manufacturing, Academic Press, Boston, MA, 1999.