

## Simple Method for Calculating Backside Via Inductance

R. Tsai, W. Okamura, P. Nam, R. Grundbacher, M. Nishimoto, Y. C. Chou, R. Lai, and S. Olson

TRW, Inc., Redondo Beach, CA 90278

Tel: (310) 812-8254, Fax: (310) 813-0418, Email: [roger.tsai@trw.com](mailto:roger.tsai@trw.com)

### Abstract

Backside via self-inductance is a critical electrical quantity needed for the design of Monolithic Millimeter-wave Integrated Circuits (MMIC). We have investigated a simple, analytical method for accurately calculating via inductance based upon physical geometry. The analytical method enables backside via process development to be tailored to meet design goals. Conversely, the sensitivity of RF performance yield to via process variation can also be evaluated.

### INTRODUCTION

The backside via is an essential and ubiquitous element in MMIC technology. Although a via offers a low resistance contact to the grounding plane, its self-inductance is a critical electrical parasitic that can severely degrade circuit performance at high frequencies. Therefore, the via should be engineered to reduce its inductance to acceptably low levels.

However, with the recent explosion in the demand for MMICs, the needs to reduce cycle time and increase wafer substrate size have become dominant factors in process development. As a result, traditional etching systems are being supplanted by new, higher etch rate systems for 4" and 6" GaAs wafers [1]. These new etching systems not only offer higher etching rates, but also produce vias with much higher aspect ratios. This is demonstrated in top and bottom photographs of Figure 1, which show cross-sectional views of vias from TRW's 2-mil GaAs process that were etched in our current production system and one such new, high aspect ratio system.

Unfortunately vias with higher aspect ratios also have higher self-inductance. Thus, there is a great need to balance these via processes between high throughput and low inductance, or lower aspect ratios. We have investigated a simple, yet accurate method for calculating via inductance based only upon its physical geometry. Our method uses a simple, analytical equation based on basic electrostatic physics. With this method, forward engineering of the via process to meet MMIC design specifications can be done quickly and easily, or conversely, reverse engineering the effect of physical via variation on circuit performance can also be performed.

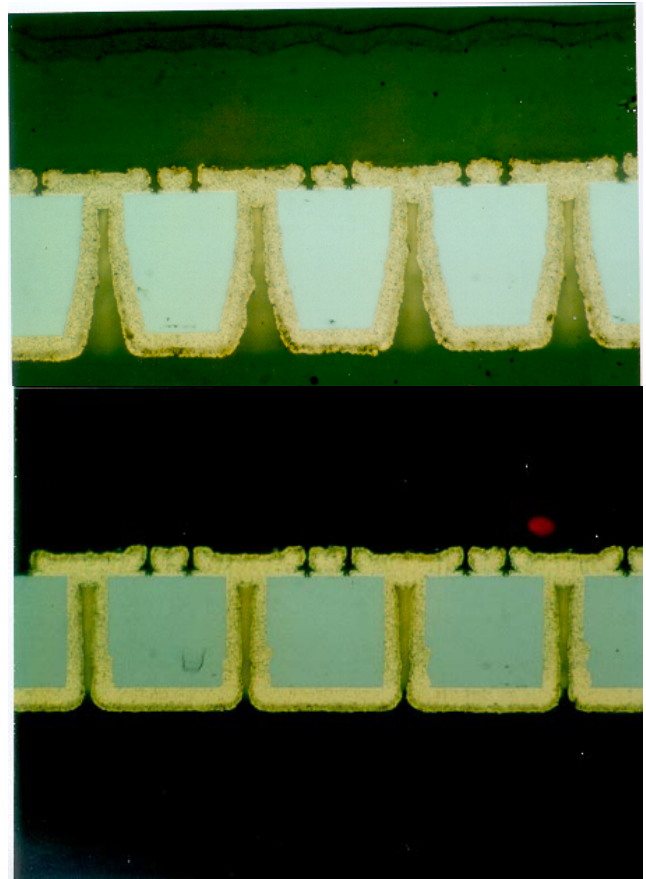


Fig. 1 (Top) Cross-section of 2-mil GaAs via etched with old system.  
(Bottom) 2-mil GaAs via etched with new system.

## SIMPLE METHOD

In order to assess the trade off between via geometry and parasitic inductance, an accurate means of relating the two must be established. We have evaluated the results of electromagnetic simulation as well as measured electrical and physical verification in establishing our analytical relationship.

Electromagnetic (EM) simulation is widely used in millimeter wave IC design. Commercial EM tools such as SONNET Software's EM and Agilent's HFSS are routinely used at TRW to accurately simulate the electrical characteristics of circuit interconnects. EM simulations clearly show that as the aspect ratio of a via increases, so too does its self-inductance. This can be demonstrated through an EM simulation of TRW's 2-mil GaAs via using SONNET's EM. TRW's 2-mil via, which is nominally cylindrical, was approximated to a rectangular pyramidal shape in the example EM, as shown in Figure 2. Although not exactly representative of the via, the simulation accurately portrays the relationship between aspect ratio and inductance. As shown in Table 1, as the aspect ratio is varied between 1.73 (30° slope) and perfect vertical, the self-inductance changes 50%, from 12 pH to 18 pH.

Table 1. EM simulated Via Self-Inductance

Top Width (μm)	Top Length (μm)	Θ (degrees)	L (pH)
40	30	20	8.9
25	15	15	15
30	20	15	13
35	25	15	11.1
25	15	0	18.2
25	15	30	12.2

For simplified via geometry, such as a perfectly round cylinder with vertical slopes, simple electrostatic principles can be used to form a closed-form, analytical solution for self-inductance. In the case of the perfect cylindrical via, Pucel has offered such a solution [2]:

$$L \equiv \frac{\mu_0}{2\pi} \left[ h \left( \ln \left( \frac{h + \sqrt{r^2 + h^2}}{r} \right) \right) + \frac{3}{2} \left( r - \sqrt{r^2 + h^2} \right) \right] \quad (1)$$

where  $r$  is the radius of the cylinder,  $h$  is the substrate thickness, and  $\mu_0$  is the permeability of free space.

We have found that this closed-form expression can be modified to work for general cylindrical vias, including those that are more oval and have a nonzero aspect ratio. By including an empirical correction factor that is a function of sidewall slope (aspect ratio), we have been successful in generalizing (1):

$$L \equiv \frac{\mu_0 A}{2\pi} \left[ h \left( \ln \left( \frac{h + \sqrt{r'^2 + h^2}}{r'} \right) \right) + \frac{3}{2} \left( r' - \sqrt{r'^2 + h^2} \right) \right] \quad (2)$$

where  $r'$  is the effective radius of the new via, and  $A$  is an aspect ratio dependent correction factor given by:

$$A \equiv A_0 \left( 1 - \frac{\Theta}{90^\circ} \right) \quad (3)$$

$$\Theta \equiv \cot^{-1}(AR) \quad (4)$$

$$AR \equiv \frac{h}{\Delta r} \quad (5)$$

where  $\Delta r$  and  $\Theta$  are shown in Figure 3, and  $A_0$  is an empirical shape correction factor

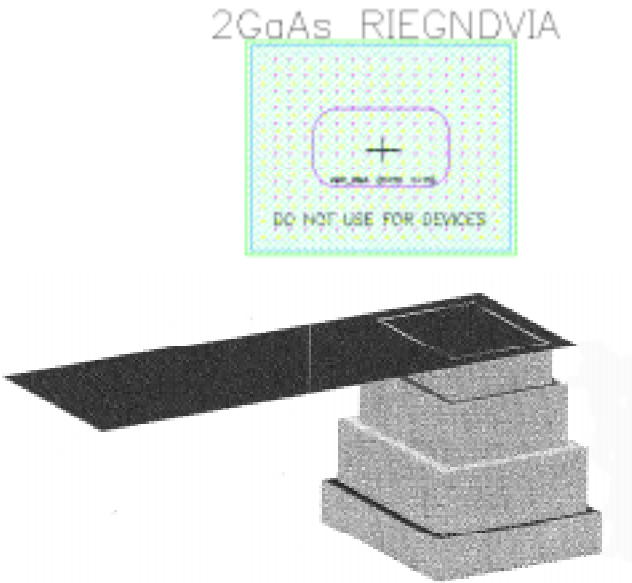


Fig. 2 (Top) Top view of 2-mil GaAs via.  
(Bottom) Rectangle approximated geometry of EM simulation.

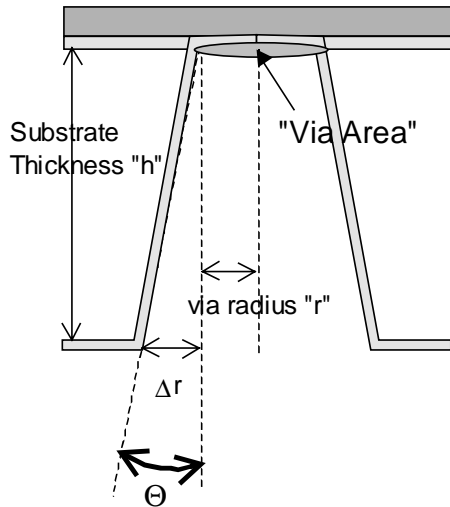


Fig. 3 Backside Via diagram.

In the new relationship (2), the effective radius is the radius of a circle that is of equivalent area to the new via's top contact area, as shown in Figure 3, while  $A_0$  is a factor that must be determined for the shape of the top contact. For example, in the case of the  $25 \times 15 \mu\text{m}$  rectangular top contact area in the EM simulation example above,  $r'$  would be  $10.925 \mu\text{m}$ , while  $A_0$  was determined to be 1.8 for rectangular areas. Note that  $A_0$  would be 1 for perfectly circular areas.

## RESULTS & DISCUSSION

With the new analytical expression for via inductance, inductance can quickly and easily be calculated for a wide variety of via shapes, without the need for extensive EM simulation. For example, (2) can be used to fully express the EM simulated inductance for the cases in Table 1, as shown in Figure 4.

The new method has been shown to work very well for calculating the inductance of TRW's various backside via technologies. For example, (2) accurately calculates the via inductances that are used in MMIC design for TRW's production 2-mil & 4-mil GaAs HEMT processes, as shown in Figure 5. These production vias are described in Table 2, and have been well characterized through cross sections like the ones shown in Figure 1 and Figure 6 for 2-mil & 4-mil vias, respectively. In addition, (2) has also accurately calculated inductances that have been extracted for 2-mil GaAs via experiments employing the new, high aspect ratio etching system, as described in Table 2 and also shown in Figure 5.

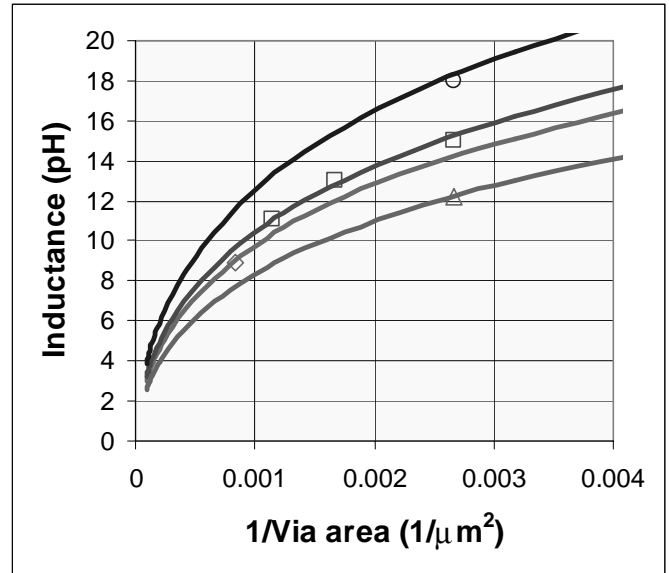


Fig. 4 Accurate calculation of EM simulated via inductances using simple analytical expression (2).

Lines: calculated with (2):  
 Slope =  $0^\circ$ , Slope =  $15^\circ$ , Slope =  $20^\circ$ , Slope =  $30^\circ$ ;  
 Points: EM-simulated:  $\circ$  Slope =  $0^\circ$ ,  $\square$  Slope =  $15^\circ$ ,  $\diamond$  Slope =  $20^\circ$ ,  $\triangle$  Slope =  $30^\circ$

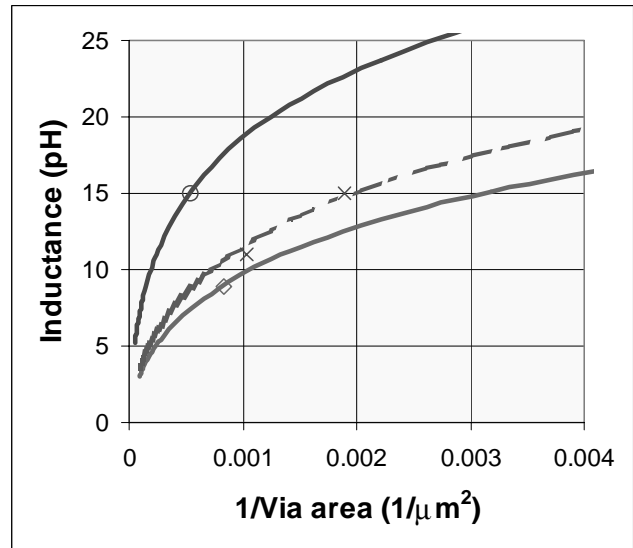


Fig. 5 Accurate calculation of design/extracted via inductances using Simple analytical expression (2).

Lines: calculated with (2):  
 2-mil GaAs w/ old system, 4-mil GaAs w/ old system, 2-mil GaAs w/ new system;  
 Points: Extracted:  
 $\square$  2-mil GaAs w/ old system,  $\diamond$  4-mil GaAs w/ old system,  $\times$  2-mil GaAs w/ new system

Table 2. Backside Via descriptions

Backside Via	Top Contact	$\Theta$ (degrees)	L (pH)
2-mil GaAs old	~ rect. 40x30 mm	20	8.9
4-mil GaAs old	Circle 50 mm diam	17	15
2-mil GaAs new	~ rect. 28.5x18.5 mm	7.5	15
2-mil GaAs new	~rect. 36.5x26.5 mm	7.5	11

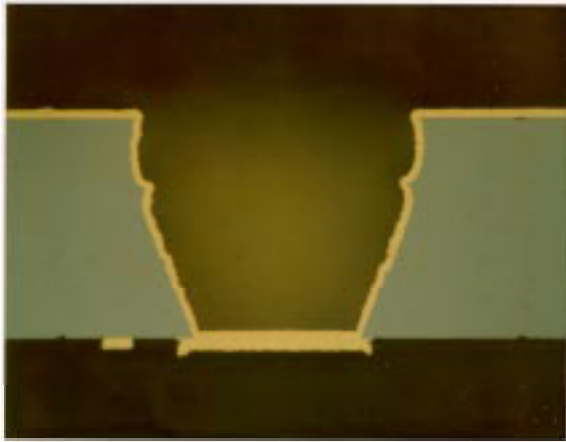


Fig. 6 Via cross-section of 4-mil GaAs via, etched w/ old system.

## CONCLUSIONS

TRW has investigated a simple, analytical method for calculating the inductance of backside vias. The method is based on general geometric parameters that describe most backside via shapes. The method provides results that are easy to derive, yet valuable for forward engineering.

## ACKNOWLEDGEMENTS

The authors would like to thank all managing and support staff in TRW's Semiconductor Product Center. Even our most advanced technologies would never succeed without their efforts.

## REFERENCES

- [1] R. Szveda, Production Etch Processing for GaAs, III-Vs Review, vol. 13, no. 5, pp. 48-52, Sept/Oct 2000
- [2] R. Pucel, Modeling Via-Hole Grounds in Microstrip, IEEE Microwave Guided Wave Lett., vol. 1, no. 6, pp. 135-137, June 1991.