Reversible and Permanent Wafer Bonding for GaAs Processing

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Abstract

Wafer bonding for Compound Semiconductor processing is a new manufacturing technology, which is highly appreciated by the industry and supports successfully new ways of processing thin and large diameter GaAs wafers.
GaAs wafers temporarily and reversibly bonded to a carrier substrate are suited for reliable back thinning and backside lithography. Permanent wafer bonding allows the production of Si/GaAs wafer heterostructures for the integration of optoelectronic devices into Si integrated circuit (IC) technology.
This paper will describe two state-of-the art methods and corresponding results of wafer bonding for manufacturing thin and therefore fragile GaAs wafers:

(a) Aligned reversible wafer bonding to a rigid carrier substrate by wax for optimum handling during production;
(b) Permanent bonding to a Si wafer via an epoxy or glass-like interlayer.

1. Introduction

Wafer bonding is the key enabling technology for the production of MEMS and MOEMS (micro-electro- and micro-opto-electro-mechanical systems)[1,2] as well as for large scale SOI (Silicon-On-Insulator)[3,4,5] applications. In MEMS/MOEMS the most widespread permanent wafer bonding techniques are anodic bonding, fusion or silicon direct bonding and thermo-compression bonding. The latter utilizes interface layers of glass frit, metals for eutectic bonding or adhesives. For SOI wafer fabrication a reversible hydrophilic bond between a bare Si wafer and an oxidized Si wafer is established. In the subsequent annealing process at approx. 1100°C the reversible bond is transformed into a permanent bond.
Wafer bonding for Compound Semiconductors is a new bonding application which has the potential to establish itself as key enabling technology. In this paper two important areas of applications for GaAs are presented.

2. Reversible Wafer Bonding Using Wax

GaAs and other III-V material processes require back thinning and backside lithography. The execution of such production steps is a quite delicate procedure or even impossible due to the enormous fragility of such materials.
One solution to master these handling problems is reversible wax bonding. Here the III-V device wafer is coated uniformly with wax and then bonded to a carrier substrate. After bonding the handling of the device wafer for back thinning and backside lithography can be performed without any problems. The use of a carrier substrate improves the mechanical strength while the wax reliably bonds and further protects the active surface of the device wafer during grinding and polishing. This type of bonding is termed reversible because device and carrier substrates can be de-bonded quite easily once back thinning and backside lithography has been completed.
As carrier substrates either quartz, glass or even Si wafers are commonly used.
A Fully Automated Wax Bonding System of EV Group (www.EVGroup.com) has been utilized for wax coating and reversible bonding processes.
Fig. 1 shows a photograph of such an equipment with a close-up of the proprietary wax coating module.
Fig. 2 shows the typical process flow and a principle layout of an integrated cluster-like wax bonding system.

- Device wafers and carrier substrates are stored in individual cassettes for automated loading.
- After optical pre-alignment, the device wafers are coated in a special coating module. The wax is dispensed at elevated temperatures onto the active device wafer surface. Special technical tools used are heated dispense lines, special dispense pumps as well as a heatable spinner chuck. The thickness of the deposited wax coating is in the range of 20 µm up to 100 µm. Fig. 3 shows the thickness uniformity of a typical wax layer across a 6" GaAs wafer. The target thickness was 45 µm with a remarkable uniformity of better than ± 4%. Notice that the uniformity will be further improved during the bonding process.
- After coating, device and carrier wafers are loaded into the bond chamber by the robot where they are precisely aligned to each other. Special technical means serve for the

fine alignment since carrier substrate and device wafer may have different sizes.

- The bonding procedure is fully software controlled. After bonding the wafer pair is loaded into a receive cassette.

Further processing steps include back thinning of the device wafer and back-side lithography.

The bonding force exerted by the wax interlayer is strong enough to withstand the subsequent wafer grinding and CMP polishing.

For lithography the wafer is coated with photoresist, aligned to the photomask, and exposed.

The latter production steps require a Mask Aligner of type EV620 CS (specifically tooled for compound semiconductor application) of EV Group. This Mask Aligner is equipped with special optical means in order to perform backside precision alignment. Since the bottom side microscope has to view through the transparent carrier substrate onto the active device wafer surface the depth of focus of the Mask Aligner has to be switchable. This is performed by utilizing the most accurate and repeatable Z axis of the alignment stage instead of refocusing the microscope.

Fig. 1: Wax Bonder with coating module and heatable chuck

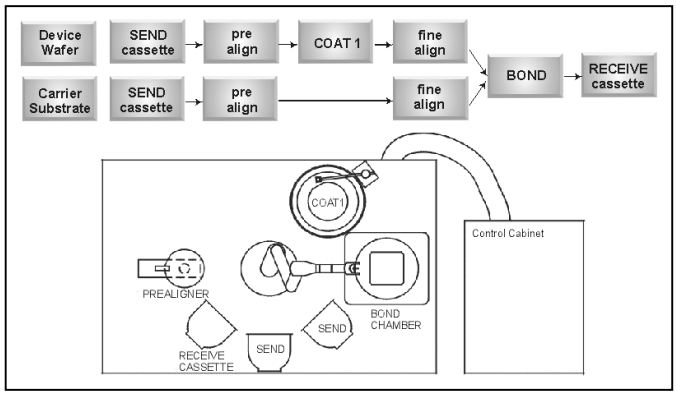

Fig. 2: Process flow for automatic wax coating and bonding and schematic top view of the Wax Bonding System

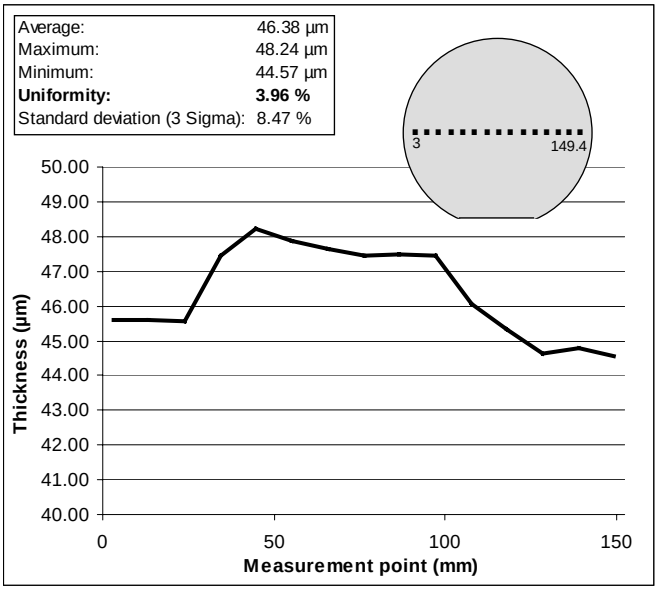

Fig. 3: Results on wax coating of 6" GaAs wafer: thickness uniformity

3. Permanent Wafer Bonding for GaAs/Si Heterostructures

3.1 Background:

Integration of GaAs optoelectronic devices into silicon integrated circuits is of considerable technological interest. One of the main demands for the integration is to fabricate high quality single crystalline GaAs layers onto silicon substrates. The GaAs/Si heterostructure would have the advantage of combining the properties of both Si and GaAs and allowing the integration of GaAs optoelectronic devices and the silicon signal processing devices on the same chip and also allowing a higher power dissipation due to the three times higher thermal conductivity of silicon[6].

One possible approach is to produce a thin GaAs layer with bulk quality on a Si substrate. Usually, GaAs layers are epitaxially grown on Si substrates. In this case, the formation of antiphase boundaries, 4.1% lattice mismatch between GaAs and Si and low temperature epitaxy are major problems encountered[7,8]. Most of these problems can be avoided by using a direct wafer bonding (DWB) technique to fabricate GaAs/Si heterostructures[9,10]. Moreover, by DWB it is possible to transfer a single-crystalline (100) GaAs layer on a Si substrate by hydrogen implantation induced splitting[11].

The main problem encountered with bonding of GaAs to Si or oxidized Si is the large difference between the thermal expansion coefficients (TEC) of Si and GaAs (the TEC of GaAs is almost double than of Si)[12,13,14]. This can lead to de-bonding at thermal annealing over 160°C, the restriction to such a low annealing temperature leading to a low surface energy of about 0.20 J/m² [11,14]. This problem can in principle be solved by using silicon on sapphire wafers instead of simple silicon wafers[15]. Other groups are working in the integration of silicon in GaAs technology by transferring a silicon layer on GaAs by wafer bonding [16].

In this paper direct bonding of GaAs to Si using a Spin-On-Glass (SOG) intermediate layer is proposed. The spin-on deposition is very simple by comparison with low pressure chemical vapor deposition[17], e-beam evaporation[18] or spray pyrolysis[19]. SOG is a standard SiO_2 glass extensively used in microelectronic processing and does not contain electronically undesirable elements like sodium[17] or dopants like boron[17,19].

3.2 SOG-Film Deposition Process:

Spin-On-Glass (SOG) films were coated on Si using a standard sol-gel procedure. The deposition consists of the following steps:

- static dispense of the liquid SOG on the Si wafer
- spreading at 1000 rpm for 5 s
- spinning at 1000 – 5000 rpm for 100 s in order to obtain the expected gel film thickness
- drying off the solvent by spinning at 2000 rpm for 30 s
- pyrolysis of the gel film in ambient atmopshere at temperatures between 150°C – 180°C.

3.3 DWB of GaAs/Si via SOG Intermediate Layer:

The process described in section 3.2 was applied to investigate the GaAs/Si heterostructure system[20].
SOG layers were deposited on Si wafers as described.
Samples were prepared by coating a 370 nm thick SOG layer onto p-type (100) oriented Si wafers. These wafers were then bonded to (100) oriented GaAs wafers at RT.
The surface energy of samples bonded at RT was about 400 mJ/m², which is high compared to Si/Si hydrophilic bonding. The bonded pairs were then annealed at 200°C and 225°C, respectively, for 10 hours. Fig. 4 shows the surface energy of three identically processed GaAs/Si bonded pairs.

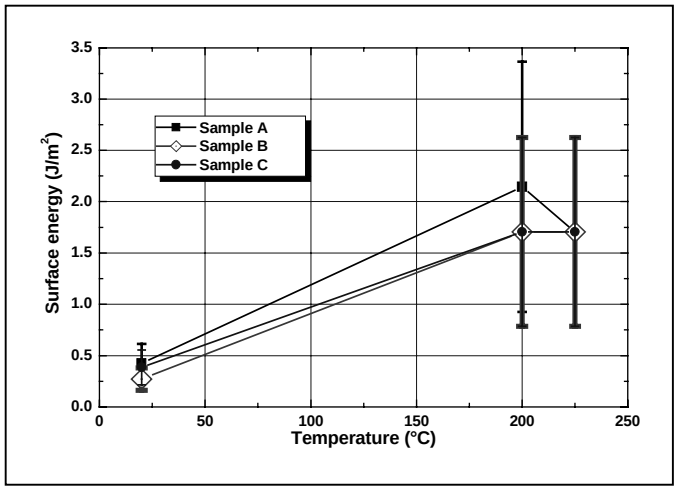

Fig. 4: Surface energy measured for three different GaAs/Si bonded pairs

After annealing at 200°C the surface energy increased to 2 J/m². Annealing at 225°C or a prolonged annealing time did not further increase of surface energy.

Due to the high thermal mismatch of the two materials (thermal expansion coefficient of GaAs is twice that of Si) the behavior of the bonded pairs during annealing was investigated by in situ measurement of the bow.
A large bow is generated during the annealing process, reaching about 500 µm at 200°C. The bow values are following the same path for heating and, thereby showing no hysteresis. The tensile strength test revealed an average value of about 22 MPa for the maximum stress.
To determine the maximum temperature applicable to the GaAs/Si heterostructure, the bow was measured during heating of the annealed bonded wafer pair. At temperatures above 280°C the wafers de-bond and/or shatter.
Fig. 5 shows the IR transmission image of a GaAs/Si bonded pair. A good quality interface can be observed, without any enclosed bubbles.

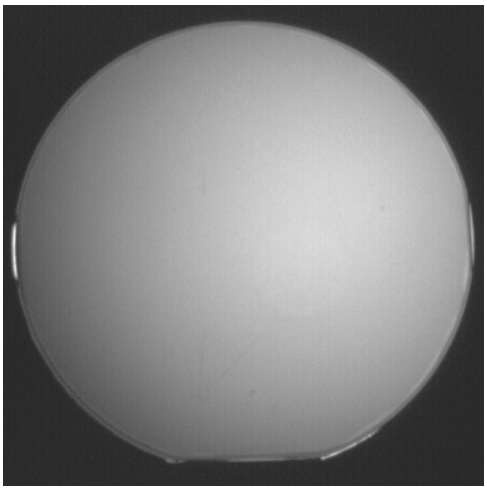

Fig. 5: IR transmission image of a GaAs/SOG/Si ComBond wafer after annealing at 200°C/10 h

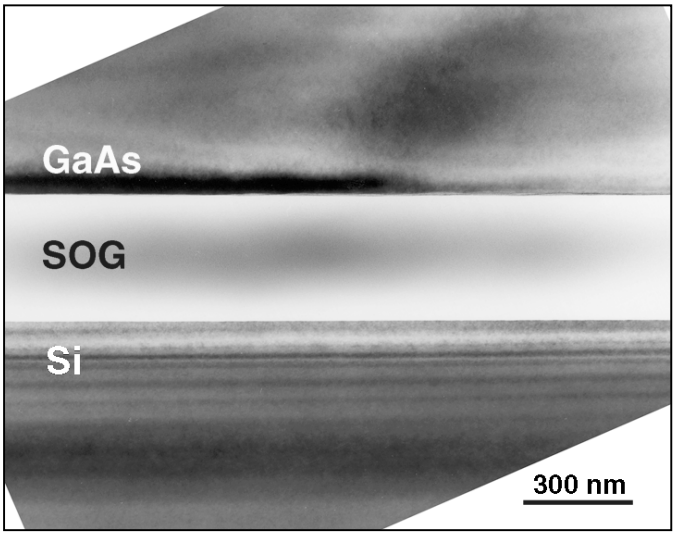

Fig. 6: Cross sectional TEM image of the GaAs/SOG/Si ComBond wafer interface

A good thickness homogeneity of the SOG layer and high-quality GaAs-SOG and SOG-Si interfaces have been observed (see Fig. 6).

Similar to the Si/Si bonding via SOG intermediate layer, some GaAs/Si bonded pairs were submitted to a mechanical thinning process. The GaAs wafers were thinned to 40 µm by grinding and then polished by CMP to a final thickness of 5 µm. The mechanical thinning process does not affect the interface quality.

After thinning, the GaAs/Si bonded pairs were heated at 400°C. Even at this temperature, de-bonding or bubbles generation did not occur. The contribution of the back-thinned GaAs wafer to the thermally induced stress on the heterostructure becomes negligible. The bonded pair can even withstand higher temperatures than the original GaAs/Si heterostructure.

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[20] GaAs/Si heterostructure wafers with a SOG interlayer are commercially available (ComBond wafers of EV Group).