ON THE INFLUENCE OF IMPLANT ISOLATION AND BASE CONTACT ABNORMALITIES ON THE PERFORMANCE AND RELIABILITY OF InGaP/GaAs HBTs

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ABSTRACT- **We studied the effect of both the separation between the emitter and the ion-implant isolation, and the surface roughness beneath the base contact on the performance and reliability of our InGaP/GaAs HBTs. We used a set of devices with four different separations (δ) between the emitter and the isolated region. We demonstrate that decreasing the separation δ gives rise to periphery base currents and causes a significant drop in device lifetime. For the base contact, we show that degradation in semiconductor surface quality beneath the deposited p-ohmic metal can cause collector leakage currents, which we relate to localized spikes through the collector layer.**

INTRODUCTION

The ion implantation technique is widely used in semiconductor device technology to selectively isolate devices by creating high resistivity regions on the wafer, while retaining the planarity of the structure [1]. In our GaAs HBT, ion-implant isolation is used also to reduce the base-collector capacitance, and thereby increase their high frequency response [2-3].

This technique raises some concerns related to the lateral spread of damage caused by the implant, and the requisite thermal annealing process following the implantation. In order to improve device quality, it is essential to establish how close the implant can be located relative to the active region without causing critical degradation to the device performance or its lifetime.

In this work, we report results of a systematic study of changing the separation (δ) between the emitter and the isolated region.

Alloyed base contacts in HBT devices are commonly used by depositing the chosen contact metallurgy on the top of a semiconductor and subsequently thermally annealing [4]. In our process, the contact is alloyed through the InGaP shelf to make contact to the highly doped p-GaAs base layer. The contact metalization consists of Pd-Pt-Au-Pd and gives excellent contact resistances ($< 1x10^{-7}$ Ω-cm^2).

The stability of the alloyed base contact depends on the morphology of the semiconductor surface, as well as on the alloying time and temperature. It is essential to control the semiconductor surface roughness and cleanliness in order to achieve an adequate alloy penetration while avoiding spikes through to the collector layer.

We report results on base-collector current measurements obtained on devices where two different dry-etching procedures were used before depositing the p-metal contact.

EXPERIMENT

Our standard HBT manufacturing process uses a deep implantation of He^+-ions for device isolation. Details on the device structure and fabrication processing are described in a previous work [3]. DC characterization measurements in the Gummel configuration as well as single diode measurements (Base-Emitter, BE-diode and Base-Collector BC-diode) were performed for this study, in the temperature range between 25°C and 200°C. We used a set of devices with δ=0.5μm, 1.0μm, 1.5μm and 2.0μm. For each separation, we measured devices with emitter areas of 2x2μm^2 and 6.5x3μm^2.

For an accelerated lifetime test, we used a set of 75 devices with 2x2μm^2 emitter area. The variations of base and collector currents were monitored during the stress experiment and an average lifetime was estimated for each separation δ.

Our standard etching process is a Cl_2-Ar reactive ion etch at 130 mTorr. In an effort to improve production capacity by moving to more automated tool, an etching experiment was conducted under a different pressure regime using a BCl_3-He punch-through step

followed by a Cl_2-He etch process at 2 Torr. It was found that the non-standard etching process etches the exposed GaAs cap layer at roughly the same rate as the standard process, but yields a rougher surface upon which the base metal must be deposited. DC measurements were performed for this study on devices with two different emitter areas ($2x2\mu m^2$ and $6.5x3\mu m^2$) and in the temperature range between 25°C and 200°C.

RESULTS AND DISCUSSION

1- Effect of implant isolation:

Figure 1 depicts the variation of both I_b and I_c measured in the Gummel configuration on devices with $2x2\mu m^2$ emitter area and for emitter to implant separations δ=1.5μm, 1μm and 0.5μm. As one can see from this figure, both the magnitude and the ideality factor of I_b increase when δ decreases. For the closest implant separation (δ=0.5μm), I_c is also decreased, while only a slight decrease in I_c is observed for the device with δ=1.0μm. Consequently, the *dc* gain ($\beta=I_c/I_b$) decreases with δ as shown in Figure 2.

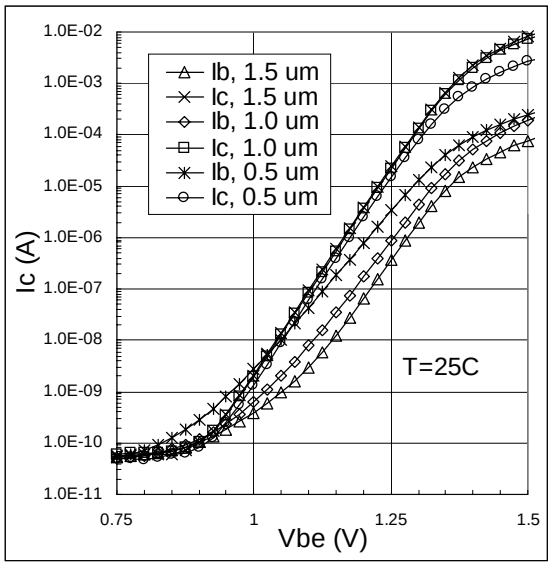

Fig. 1: Gummel plot for different emitter to implant separation δ.

Figure 3 presents the ratio between currents (I_c and I_b) measured on devices with emitter areas of $6.5x3\mu m^2$ and $2x2\mu m^2$. As one can see from this figure, the ratio of I_c for devices with δ=1.5μm agrees with the emitter area ratio (4.875). For devices with δ=1.0μm, this ratio is slightly higher (close to 5) and for devices with δ=0.5μm the ratio increases to about 5.8. This increase in I_c ratio can be explained if the physical dimension of the devices is reduced due to damage spread in the active region. In order to estimate this spread, we consider a slight variation in the emitter dimensions to obtain the effective area and periphery. Then, by assuming that the measured ratio of 5.8 is equal to the ratio of effective area for devices with δ=0.5μm, we estimate the damage spread into the active region as about 0.2μm (total spread of 0.7 μm).

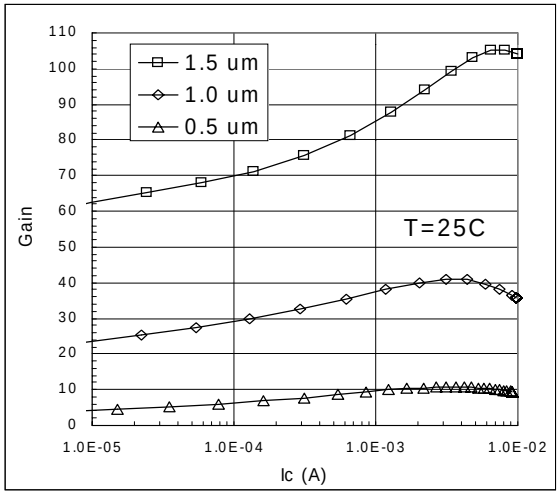

Fig. 2: Gain vs. I_c for different emitter to implant separation δ.

Moreover, when calculating the ratio of effective periphery (while considering a damage spread of 0.2μm), one gets a ratio of 2.62. This value agrees well with the I_b ratio presented for these devices in Figure 3 (for δ=0.5μm).

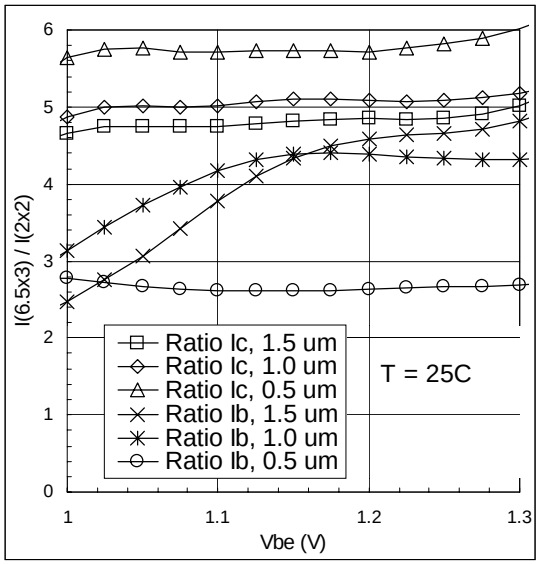

Fig. 3: Ratio of $I_c(6.5x3)/I_c(2x2)$ and $I_b(6.5x3)/I_b(2x2)$ vs. base emitter bias.

These results indicate that the base currents in this case are originated from the periphery. For the larger separations, δ=1.5μm and 1μm, the base current ratio is close to the periphery ratio at low currents, but approaches the area ratio at high currents.

We note that devices with the separation δ=2.0μm behave very similarly to those with the separation δ=1.5μm, indicating that our standard separation is adequate.

The periphery base currents were deduced separately, using the relation [5]:

$$1/\beta = 1/\beta_0 + (J_{pr}/J_c)(L/A)$$

where, β is the measured gain, β_0 is the intrinsic gain, J_{pr} is the periphery base current per unit length, J_c is the measured collector current density, *L* is the periphery, and *A* is the emitter area. The periphery current is then deduced by: $I_{pr}=L\ J_{pr}$.

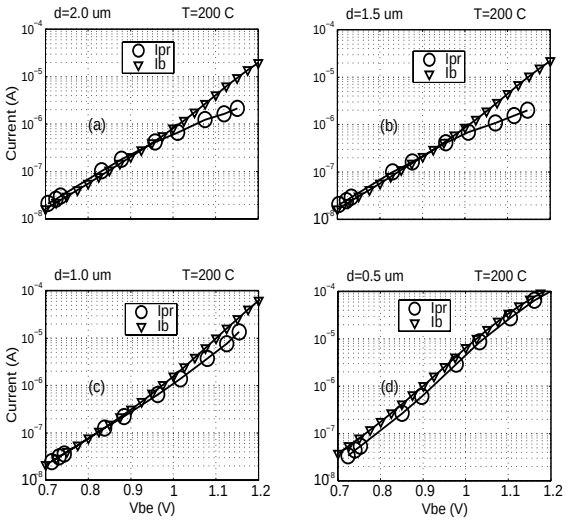

Fig. 4: Periphery current compared to measured I_b for different separations δ, at T=200°C.

Figure 4 gives the deduced periphery current I_{pr} compared to the measured I_b obtained at 200°C. As one can see from this figure, for devices with δ=1.0, 1.5, and 2.0μm, the periphery current is significant at low bias voltages, whereas for devices with δ=0.5μm, the deduced periphery current dominates the base current for the whole bias range. These results are consistent with the results obtained by current ratio in Figure 3.

For the reliability test, we monitored the degradation of the *dc* gain β with time. In this study, the lifetime is defined as the time needed to cause a drop to the *dc* gain β by 20% from its initial value before stress.

We observed that under highly accelerated aging, devices with δ=0.5μm have an average lifetime of 20-25min, whereas devices with δ=1.0μm have an average lifetime around 20h (1200min). Devices with δ=1.5μm and 2.0μm have a comparable average lifetime of around 22h (1320min).

2- Effect of surface roughness after dry etching:

Figure 5 presents the measured BC-diode current at different temperatures between 25°C and 200°C, obtained after a standard etching procedure.

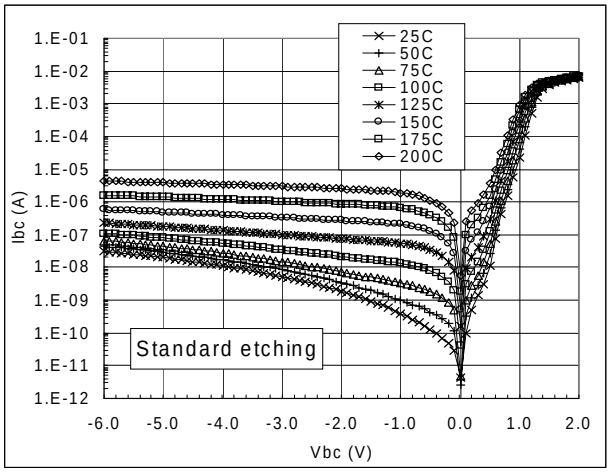

Fig. 5: Base-collector I-V vs. temperature, for devices with 2x2μm^2 emitter area. Standard etching conditions.

As one can see from this figure, at reverse biases the current is strongly dependent on temperature.

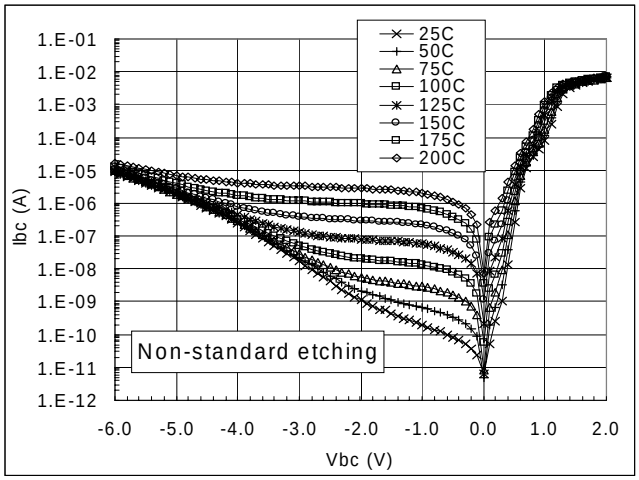

Fig. 6: Base-collector I-V vs. temperature for devices with 2x2μm^2 emitter area. Non-standard etching conditions.

Figure 6 presents measured BC-diode currents at different temperatures between 25°C and 200°C, obtained after the non-standard etching procedure.

At reverse biases < 2V, one sees also a thermally assisted current, similar to that observed in the case after standard etching (see Figure 5) and with a comparable magnitude. At reverse biases > 2V, a strong tunneling component of the current is present, which depends very weakly on temperature.

We find that the ratio of currents between the different sizes is quite arbitrary, with no dependence on either area or periphery. Furthermore, we also observed that the magnitude of the measured tunneling currents has a random spatial distribution on the sampled wafers.

These results bring us to the conclusion that the tunneling currents are localized. One of the possibilities is that the origin for these currents lies in spiking of the alloyed base contact through to the collector. Due to the sharpness of such a spike, the electric field might be high enough to favour tunneling.

CONCLUSION

It was shown that decreasing the separation between emitter and implant causes radical degradations in the device performance and reliability. For the closest implant separation (δ=0.5μm), the damage penetrates into the active region of the device and decreases its effective area. We demonstrated that for δ=0.5μm, the base current originates from a periphery source. Under highly accelerated stress conditions, the average lifetime of devices with δ=0.5μm is lower by more than a factor of 60 compared to that of devices with δ=1.0μm. The gain for δ=0.5μm dropped by a factor of 4 compared to that of δ=1.0μm. By increasing δ from 1.0μm to 1.5μm, the gain increased by a factor of 2.3 and the lifetime increases by a factor of 1.1. For devices with δ>=1.5μm, we observed very comparable performance and reliability characteristics.

It was shown also that changing the etching conditions before depositing the p-ohmic contact could have a considerable impact on the forward and reverse I-V characteristics. On some surfaces, the reverse current displayed a large tunneling contribution, which we attribute to ohmic spikes caused by rough etched surfaces.

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