# Applications of Compound Semiconductors in High Data Rate Optic Fiber Communications

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## ABSTRACT

This talk will provide a general overview of the high speed electronics necessary to provide the essential physical layer interface between the high speed TDM optical signals and the lower bit-rate tributary electrical signals. We will examine the performance requirement of each critical function block and the associated compound semiconductor IC technologies needed to achieve an ETDM data rate of 40 Gbps per wavelength.

## INTRODUCTION

Recently the exponential rising of Internet traffic has created greatest demand on the capacity of the optic fiber links which form the backbones of the global communication networks. One solution is to use the Wavelength Division Multiplexing (WDM) technique to multiply many Electronically Time Division Multiplexed (ETDM) channels together into a single strain of fiber to boost total capacity. Under today's technology, it is capable to transmit 160 channels, each running at 10 Gbps, for an aggregated capacity of 1.6 Tbps per fiber.

However, the total capacity of the WDM technique is bounded by the available bandwidth of the in-line optical fiber amplifier which is needed to compensate the loss of long fiber span. The gain spectrum of the optical amplifier is limited by the gain media and pump lasers. The state-of-the-art bandwidth of the commonly used erbium-doped optical amplifier (EDFA) is 75 nm. The best bandwidth of the emerging Raman amplifier is 92 nm. A high capacity WDM system carries multiple channels at different wavelengths with guard bands to isolate each channel. The width of the guard band is limited by the roll-off characteristics of the optical filters. The guard band of a best realized channel filter is 25 GHz between two adjacent WDM channels. With this guard band separation, the spectral efficiency is only 28%, if we have 10 Gbps traffic running in each channel. The spectral efficiency would be increased to 60% if 40 Gbps data traffic is carried on each channel. By increasing the bit rate of each WDM channel, the number of guard bands for isolating wavelengths is reduced and the spectral efficiency is increased. The overall cost of the high bit-rate WDM terminals will also be reduced because we use fewer expensive optical components such as lasers and passive optical components. Carrying 40 Gbps per channel in a next-generation WDM system of 160 wavelengths, a total of 6.4 Tbps capacity is readily to be reached.

## OPTOELECTRONIC TRANSCEIVER

High speed electronics provided important interface between the local electronic data traffic and optoelectronic devices. The schematic diagram of a conventional 40 Gbps optoelectronic transreceiver is shown in Figure 1. In the transmitter, the tributary data streams from four local 10 Gbps data channels are fed into a multiplexer (MUX) and time-domain multiplexed (TDM) to a single serial data stream at 40 Gbps. The amplitude of this combined data is boosted by the modulator driver (MDD) to modulate the electro-optical modulator such as a LiNbO3 Marc-Zander interferometer. On the receiver side, the photo-current from the optical detector is amplified by the Trans-Impedance Amplifier (TIA) and limiting amplifier (LA) before being fed into the clock-and-data recovery

circuit (CDR). The CDR circuit recovers the incoming serial data and clock components by synchronizing the incoming data stream and local clock through phase/frequency-locked loops and voltage-controlled oscillator (VCO). The recovered data is then broken down into lower speed tributary channels with a de-multiplexer (DeMUX).

Different categories of high speed ASICs are used in the transceiver, such as analog, digital and mixed-mode ICs. Analog ICs such as trans-impedance amplifier (TIA), modulator driver (MDD) and voltage-controlled oscillator (VCO) with operating frequency as high as the bit-rate are needed to handle the high speed serial data stream with minimum distortion and jitter generation. High speed digital logics are also needed to perform multiplexing and de-multiplexing functions with fast switching speed and minimum timing ambiguity. The phase-locked loop (PLL) in the CDR is critical to reproduce the clock and data from the received serial data stream.

High Speed IC Technologies

Extremely high bit-rate transmission experiments up to 320 Gbps have been demonstrated in silica fiber with Optic Time-Domain Multiplexing (OTDM) techniques with all-optical multiplexing and de-multiplexing techniques [1]. Electronic Time-Domain Multiplexing (ETDM) techniques still have many advantages over OTDM because electronic devices continue to enjoy high functionality, small size, low cost and high reliability.

The speed of electronic circuit is limited mainly by the cut-off frequency of transistors. Typically, the current gain cut-off frequency, $f_T$ , and the maximum oscillation frequency, $f_{max}$ , are commonly used figure-of-merits of an IC technology. The $f_T$ is a good indicator of the switching speed of logic circuits while the $f_{max}$ is a good measure of analog circuits. In order to choose a proper IC technology to provide fast enough switching speed and proper system margins, a transistor technology with $f_T$ and fmax better than four times of the bit rate is preferred to implement high speed ASICs. Novel circuit technologies such as distributed design and the use of multiple phase half-rate clocks are able to reduce the cut-off frequency requirement to twice of the bit-rate.

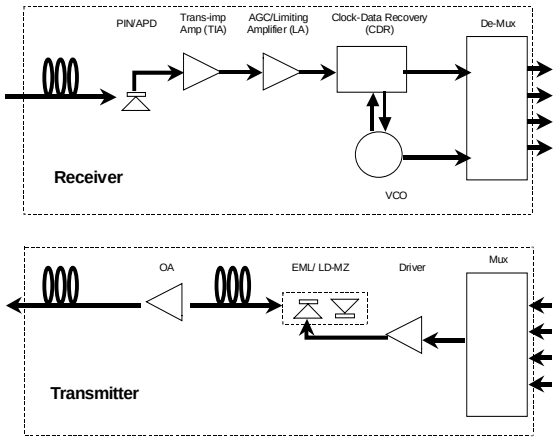


Figure 1 The schematic diagram of a generic opto-electronic transceiver.

The $f_T$ of field-effect transistors, such as MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), GaAs MESFET and GaAs or InP HEMTs, is limited by the carrier transit delay in the gate region. This transit time is determined by the lateral dimension of the gate electrode and by the electron velocity in the host material. The $f_T$ of these FETs can be increased by the scaling of the gatelength with advanced lithography tools. However, the cut-off frequency of bipolar transistors, such as silicon bipolar transistor (BJT) or the heterojunction bipolar transistor (HBT), is determined mainly by the vertical layer thickness and less by the lateral dimensions.

If we keep track the cutoff frequencies for generations of IC technologies over years by recording the best $f_T$ data from research laboratories and typical $f_T$ data in production lines year-by-year, Figure 2 shows very interesting trends. The performance of transistors improves every year mainly from the advances of fine-line lithography tools. Using the same technology in a given year, exotic materials with better electronic properties such as GaAs, SiGe and InP produce faster transistors than the main stream silicon CMOS devices. It is also interesting to see how IC technologies of physical layer ASICs are evolved for each generation of SONET standard. Taking the OC48 product development as an example, it

was launched in the late 1980's using GaAs MESFETs and silicon BJTs. Both were ready in the early production stage with enough $f_T$'s in the 10 GHz regime for the 2.5 Gbps data rate. As the performance of the production CMOS technology was ready in the late-1990's, most of the OC-48 ASICs were ported to the advanced CMOS technology for lower cost, lower power consumption and higher integration scale.

The evolution of ASIC technology roadmap for several SONET generations can be summarized in Figure 3. Today, most of the 10Gbps ASICs have been implemented on GaAs and SiGe technologies with 0.5 μm line width and is being ported to the advanced 0.16 μm CMOS technology. The 40 Gbps ASICs are still in the early stage of development to this date. Many advanced technologies such as 0.1 μm GaAs P-HEMT, 0.1 μm InP HEMTs, GaAs HBTs, InP HBTs and SiGe ICs are actively being evaluated for 40 Gbps ASIC applications.

Nevertheless, not a single technology is capable of performing all circuit functions and meeting all of the necessary requirements to construct a 40 Gbps transceiver. It is very common to employ a combination of several ASIC technologies are needed to build a transceiver module. For 40 Gbps ASICs, it is preferred to use bipolar technologies such as InP HBT or SiGe HBT to realize low power high speed digital circuits with high transistor counts and to employ GaAs HEMT or InP HEMT for analog functions which require low noise amplification and high voltage driving capability. In this talk, several practical implementations and design consideration of these ASICs will be reviewed.

[1] B. Mikkelsen, G. Raybon, R-J Essiambre, A. J. Stentz, T. N. Nielsen, D. W. Peckham, L. Hsu, L. Gruner-Nielsen, K. Dreyer, and J. E. Johnson, "320Gbps Single-Channel Pseudolinear Transmission over 200 km of Nonzero-Dispersion Fiber," IEEE Photonics Tech. Lett., vol. 12, no. 10, pp. 1400-1402, 2000.

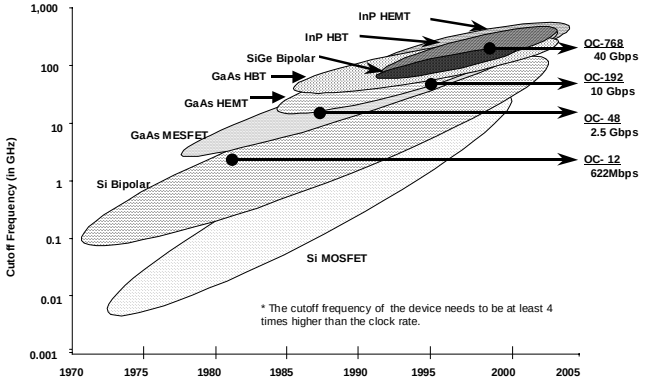


Figure 2 Semiconductor technology roadmap for lightwave electronics.

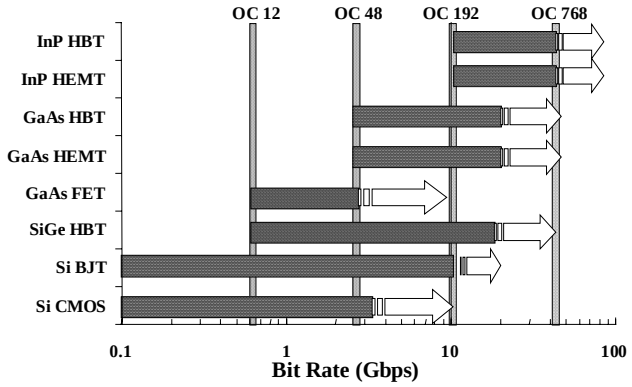


Figure 3 High speed ASIC technology for several generations of lightwave communication ASICs.