

Incorporation of an Alloy-Through Passivating-Ledge Process into a Fully Self-Aligned InGaP/GaAs HBT Process

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Abstract

Alloying base contacts directly through an InGaP emitter layer provides excellent passivation of the GaAs base in HBTs. Processes which utilize this ledge formation scheme and a self-aligned, wet-chemical base-collector etch can suffer degradation in DC performance. Layouts with a hexagonal emitter can circumvent any DC performance degradation because the base electrode can be used as the etch mask on all sides of the device.

INTRODUCTION

As InGaP/GaAs HBTs have emerged as a manufacturable technology suitable for a wide array of high-frequency and high-power applications in recent years, many published reports have focused on passivating the GaAs surface with a wide bandgap emitter ledge. A passivating ledge increases current gain β in small-area devices, lowers 1/f noise, and improves device reliability.

Several methods of ledge formation have been proposed, including using a separate lithography step to define the ledge dimensions [1], incorporation additional etch-stop layers into the epitaxial structure and exploiting selective wet chemistry [2], and alloying base electrodes directly through a thin, wide-bandgap emitter layer [3]. This last technique, here referred to as alloy-through passivation, is attractive because it requires no special epitaxial layers or process steps. Previously reported data has demonstrated that the alloy-through passivation technique can be used to fabricate HBTs with high β without sacrificing RF performance [4].

Recent work at the University of Illinois at Urbana-Champaign (UIUC) has focused on incorporating alloy-through ledge passivation into an established, manufacturable HBT process [5] which includes a self-aligned, wet-chemical base-collector etch process. A self-aligned wet collector etch improves RF performance by reducing parasitic base-collector capacitance, and can be used in aggressive high-frequency HBT processes to completely remove extrinsic collector material [6]. This work demonstrates that deleterious effects on HBT DC performance can arise from the self-aligned base-collector etch step in devices with an alloy-through ledge. This paper also presents simple layout

changes which solve this problem, resulting in approximately 50% increase in β and a tenfold decrease in output conductance.

DEVICE FABRICATION

The InGaP/GaAs epitaxial layers were grown by low-pressure MOCVD. The key features of the epitaxial structure were a 300 Å InGaP emitter ($N = 5 \times 10^{17} \text{ cm}^{-3}$), a 500 Å C-doped base ($p = 4 \times 10^{19} \text{ cm}^{-3}$), and a 4000 Å GaAs collector ($n = 2 \times 10^{16} \text{ cm}^{-3}$). A single wafer was then cleaved into pieces, with one piece processed without an emitter ledge (sample A), and two other pieces processed with an alloy-through passivation ledge (samples B and C).

Self-aligned high-frequency devices in a standard two-mesa design were fabricated using contact alignment, standard lift-off techniques for metalizations, and all wet chemical etching. A TiPtAu emitter contact was used to mask the emitter etch. The $\text{In}_x\text{Ga}_{1-x}\text{As}$ emitter cap was etched in a citric acid-based solution, which stopped on the InGaP emitter and undercut the emitter contact. The InGaP emitter was then selectively etched from sample A using HCl, but left on samples B and C. The effective emitter-to-base spacing, also the ledge length on samples B and C, was 0.25 μm . Self-aligned base contacts were then deposited: TiPtAu (150 Å, 150 Å, 1000 Å) on sample A, and PdPtAu (300 Å, 300 Å, 700 Å) on samples B and C.

The next step in the process flow was the self-aligned base-collector etch, which used the base electrode as the etch mask. The GaAs base and collector material in sample A was etched with a citric acid based solution, and an InGaP etch stop was removed using HCl. For samples B and C the etch sequence consisted of an HCl based etch to remove the InGaP emitter, a citric acid-based base-collector material etch, and an HCl based etch to remove an InGaP etch stop. The etch for sample B was straight HCl, which is known to rapidly etch laterally beneath a photoresist mask. The etch for sample C was $\text{HCl}:\text{H}_3\text{PO}_4:\text{H}_2\text{O}$ (1:3:1), which etches InGaP without appreciably undercutting a photoresist mask. The HBT fabrication flow was completed with mesa-isolation, AuGeNiAu collector contacts, alloy, polyimide planarization, and a TiAu metallization for cascade probing.

Two styles of device layout were investigated. The first is a standard UIUC layout for a self-aligned transistor, shown

schematically in Fig. 1(a). The base electrodes are deposited on two sides of the emitter, and subsequently serve as the etch mask for most of the base-collector junction area. However, photoresist used to protect the emitter material also overlaps the base material along the edges without base metal. The second layout style, which employs a hexagonal emitter, is shown schematically in Fig. 1(b). The hexagonal emitter ensures that an adequate self-aligned etch can occur on all sides of the emitter electrode, so that base metal can be deposited on all sides of the emitter without increasing base-emitter leakage currents [7]. Photoresist which protects the hexagonal emitter during the base-collector etch does not overlap any base material.

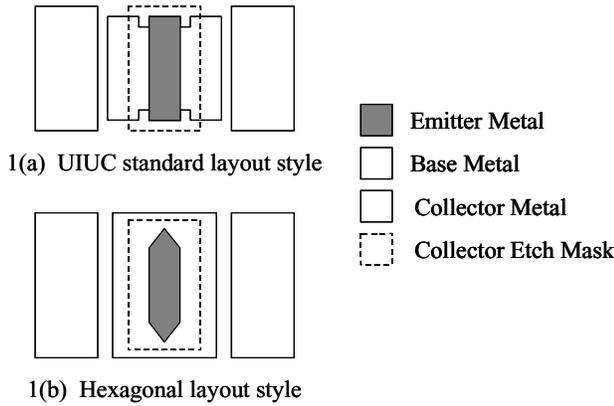


Fig 1. Standard (a) and hexagonal (b) style layouts investigated in this work.

DEVICE RESULTS

There were important differences between samples A, B, and C. First, there was no yield for self-aligned devices in sample C. The dilute HCl solution failed to completely remove the InGaP emitter ledge around the base electrodes used as the mask for the self-aligned base-collector etch, which increased the size of the base-collector mesa as shown in Fig. 2. Collector metal was subsequently evaporated and the metal overlapped the base-collector material, creating a shorted junction. More work would be required to address the problems associated with using a dilute HCl solution in a self-aligned base-collector etch step.

Although there was not a catastrophic yield problem, the DC performance for samples A and B did depend on device layout. Figure 3 shows DC current gain β for different layouts for sample A (non-ledge) and sample B (ledge). For sample A, β decreases predictably for small area devices. The hexagonal layout devices in sample B had β essentially identical to that of a large area device, indicating that the InGaP ledge adequately passivated the GaAs surface. However, the devices with a standard layout on sample B, showed a degradation in β similar to the non-ledge sample.

The standard layout devices in sample B also suffered from an increase in output conductance compared to the non-ledge devices of sample A and the hexagonal devices in

sample B. I_C-V_{CE} plots demonstrating the difference in output conductance are shown in Fig. 4. The Early voltage for a low β , standard-layout ledge device is approximately 100 V. On the other hand, the early voltage on the non-ledge devices and ledge devices with a hexagonal emitter is so large that it is difficult to measure; it is at least 1 kV.

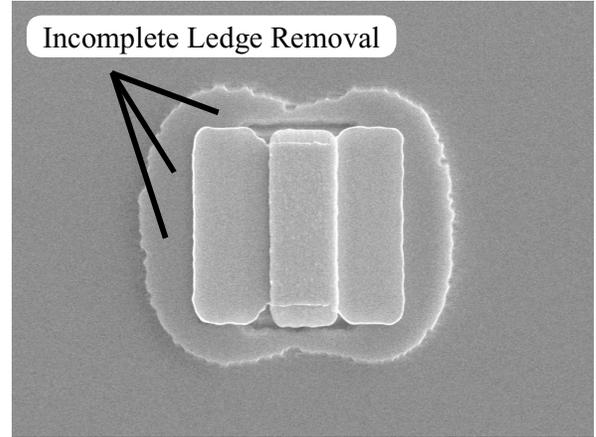


Fig 2. The increase in base-collector mesa size caused by incomplete removal of the InGaP ledge on sample C during the dilute HCl etch.

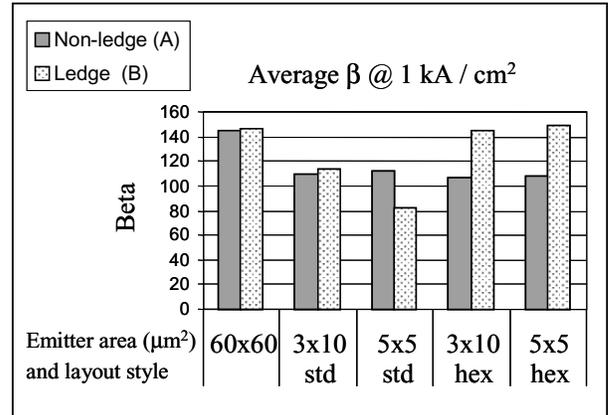


Fig 3. Beta for large and small area devices, with and without ledge.

The degradation in the DC performance of the standard-layout ledge device in sample B is attributed to problems associated with the straight HCl etch used to remove the InGaP emitter. The straight HCl rapidly undercuts the photoresist (see Fig. 1) used to protect the ends of the transistor, and the base-collector wet etch then attacks this area. SEM pictures showing the difference between standard layout devices on sample A (non-ledge) and sample B (ledge) are shown in Fig. 5. There is a small “shelf” of base-collector material in the adequately protected, non-ledge device, but this shelf is not present in the ledge device. The lack of this shelf in the standard-layout ledge device means that exposed base material is abnormally close to regions of large electric field and current flow, which the authors suggest is responsible for the observed degradation in DC performance.

The hexagonal-shaped emitter layouts use base metal on all sides of the emitter as the mask for the self-aligned base-collector etch step. Straight HCl can then be used to remove the InGaP emitter during the base-collector etch, and no problems in DC performance arise. Figures 3 and 4 show the high β and low output resistance, respectively, seen in the hexagonal layout devices on sample B.

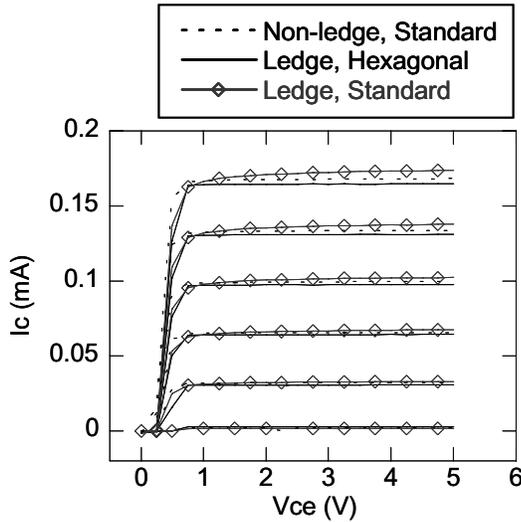


Fig. 4. I_C - V_{CE} family of curves showing the increase in output conductance on standard-layout devices fabricated with an alloy-through passivating ledge.

To further verify the passivating nature of the alloy-through ledge in hexagonal-layout devices, low-frequency noise measurements were performed on hexagonal HBTs from chips A and B. For comparison, low-frequency noise measurements were also made on devices fabricated at UIUC according to the process described in reference [2], which employ a Dual Etch-Stop Ledge (DESL) epitaxial structure. The DESL process flow leaves some GaAs base surface exposed. The noise spectral densities at 64 kA/cm^2 for typical devices from each sample are shown in Fig. 6.

The data in Fig. 6 demonstrate that, as expected, HBTs passivated with an InGaP ledge show a decrease in low-frequency noise relative to unpassivated devices. At 100 Hz, the DESL structure shows a 12 dB improvement over its unpassivated counterpart, while the alloy-through ledge sample shows a 23 dB improvement. This additional improvement in the alloy-through process is probably due to the fact that there is no exposed base surface in an alloy-through process, while the DESL process leaves some base surface exposed. It is also interesting to note that the unpassivated devices have a nearly-ideal $1/f$ dependence in the noise spectral density, while noise in the passivated devices has a more complicated frequency dependence. This is not well understood at this time.

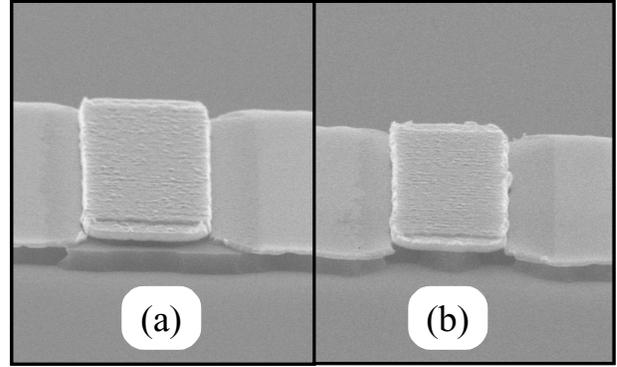


Fig. 5. SEM pictures of a non-ledge (a) and ledge (b) sample. The exposed base surface shelf in (a) has been inadvertently removed in (b), leading to degradation in DC performance.

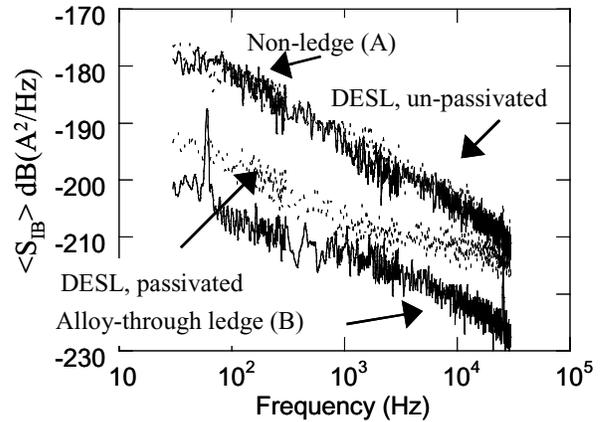


Fig. 6. Noise current spectral density of passivated and unpassivated HBTs fabricated under the DESL and alloy-through processes.

CONCLUSIONS

This paper has demonstrated the incorporation of an alloy-through ledge formation step into a fully self-aligned InGaP/GaAs HBT process. A process flow which uses a dilute HCl etch to remove an InGaP ledge as part of the self-aligned base-collector etch is inadequate due to incomplete removal of InGaP around metal features. On the other hand, a process which uses straight HCl is difficult to implement because photoresist does not adequately mask InGaP on those areas of a wafer where metal is not used as the mask. These problems are elegantly solved by the use of a hexagonal-shaped emitter. The hexagonal-shaped emitter layouts use base metal on all sides of the emitter as the mask for the self-aligned base-collector etch step, so that straight HCl can be used to remove the InGaP ledge without difficulty. Also, devices fabricated with alloy-through ledge passivation have significantly lower low-frequency noise than either unpassivated devices or devices with a ledge technique that leaves some base surface exposed.

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