150mm Through Substrate Interconnect Conversion One Year Later

L.S. Klingbeil, K.L. Kirschenbaum, C.G. Rampley, D. Young
Motorola Semiconductor Products Sector
Compound Semiconductor One; CS-1
2100 E. Elliot Road, Mail Drop EL-609 Tempe, AZ 85284
Phone-(480) 413-4147, FAX-(480) 413-5748, Email-rytk30@email.sps.mot.com

Abstract

The momentum for III-V technologies with through substrate vias continues to increase making a 150mm wafer size conversion inevitable to meet increased demands. The seven month conversion at Motorola's CS-1 was rapid and cost effective because most of the equipment set was 150mm compatible and only some additional capacity installation was needed.

The fab conversion was not without process related hurdles, including the thousand plus wafers per week run rate within the through substrate interconnect module. Maintaining a competitive wafer cost requires the minimization of resource costs which increased with the 150mm process. The increase in cost is largely attributed to increased labor force and increased sapphire mounting substrate costs. Equipment limitations processing 150mm mounted wafers and greater process sensitivity created technical challenges that required significant attention. Establishing a low cost, high volume capable process required a balance of these two constraints.

INTRODUCTION

Driven by reduced die size and increased demand for higher frequency product, the need for III-V technologies with low inductance through substrate via technology continues to increase. Rapid capacity expansion was required and the quickest, least expensive method to accomplish this was to convert from 100mm to 150mm. The seven-month wafer size conversion and additional capacity installation within CS-1 more than doubled the front and back end capacity. The conversion was not without process related hurdles, including process challenges for the one thousand plus wafers per week through substrate interconnect module. Many of the processes within this module will be explored relative to the challenges and changes relative to resources, process, and tool limitations for the 150mm through substrate via process.

PROCESS OVERVIEW

Using a high temperature thermal-plastic adhesive, the 150mm wafer is attached to a sapphire substrate using a heated, vacuum bonding machine. An automated batch wafer thickness measurement tool is used to collect thickness data throughout the thinning process. This data is automatically fed to the mechanical thinning tool and electronic data storage files. After measurement, the wafer sees a mechanical thinning process then a batch chemical polish to remove any grind damage to the surface. This process results in a final wafer thickness of 1-4 mils. Next, the photo pattern is applied to the wafer using a mask with an incorporated optical edge bead. Wafers undergo a softbake to slope the photo profile to allow some slope on the via profile. This will assist in sputtered seed metal step coverage. Using an ICP dry etch process, the through substrate vias are created. A low temperature ash removes the resist. Wet cleans are then performed for veil removal and metal preparation. Standard adhesion and seed metal layers are deposited so an electrolytic plated gold layer can be deposited.[1,2] Last, the wafer is demounted from the sapphire mount in an automated chemical hood that utilizes a unique contained wafer cell and cassette.

CHALLENGES & CHANGES

Mounting Substrates and Bonding Process

The thinning of the brittle III-V substrates to 20-100μm requires a hard mount to maintain rigidity through the backside process steps. The requirements for the mount are determined by the process used to fabricate the through substrate vias, the equipment set, and the back metal scheme. Sapphire is a common mounting substrate because it is chemically resistant and transparent for backside alignment. The cost of 150mm sapphire carriers is almost double that of 100mm carriers. This cost is exceptionally high considering the initial quantities required for both testing and running the converted module compounded with an unexpected initial 7% breakage rate. Within a few months, the breakage rate was reduced by ~4% through implementing a few new procedures. The learning curve on how to handle the larger substrate and carrier was very steep. Therefore, training on how to properly handle these expensive composites was quickly implemented.

Moreover, a modification in thermal processing at two steps in the process was implemented to reduce the exposure to sudden thermal shock. Thermal stress was not as apparent with the smaller 100mm diameter carriers triggering a new investigation. Difficulty pulling vacuum on the measurement tool hindered accurate thickness measurements. Some wafers were also failing to clamp to an electrostatic chuck. These two issues sparked the question why 100mm and 150mm reacted so differently. Each step in the process module was evaluated by performing electrostatic chuck clamping tests and composite bow measurements after each process step. An example can be seen in Figure 1. From this information the two process with large thermal stressing were determined to be the root cause. Both the thermal cycling at photolithography and the mount stages were modified to reduce the issue of bow. The reduction of bow reduced fracturing and assisted with lowering expenses.

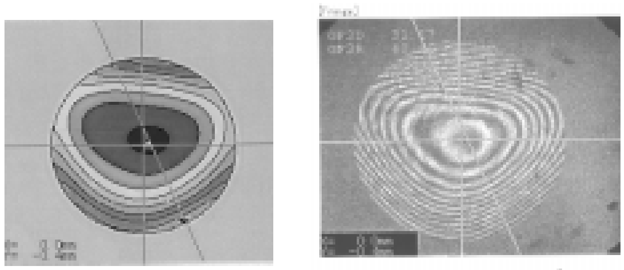

Figure 1. Composite mounted wafer stress changed significantly using 150mm substrates to the point where warp hindered accurate thickness measurements and clamping to an electrostatic chuck.

Although the sapphire breakage rate dropped, the issue of initial cost continues to contribute unfavorably to overall process wafer cost. Less expensive materials within the borosilicate glass family are currently being qualified with subtle changes to the flow for process compatibility. The price differential is close to 10X and well worth the exercise of modifying the process for compatibility.

Thinning

The wafer thinning process required considerable modification to convert from 100mm to 150mm. The tool for mechanical thinning was easily upgraded to 150mm. On the other hand, the process did need some modification. The tool used for the chemical polishing of 100mm wafers could not be converted to 150mm. Therefore, a new method of polishing needed to be developed. Since spray acid tools were available in house, it was decided to use a wet etching polishing process. A new chemistry and process needed to be developed. Also, this meant the polishing process would be transferred from a single wafer tool to a batch tool. This necessitated a change from a batch process on the mechanical thinning process to an individual wafer process. The larger surface area of the 150mm wafer made across wafer uniformity more difficult to control especially on the thinner product lines. The wafer thickness and uniformity was controlled using a combination of a wafer measurement tool and a manufacturing tool called Datalog. With the conversion, both of these controls needed significant modification.

When volumes exceed to 500, 1000, or 1500 wafers a week, manufacturing analysis tools quickly identify the measurement steps as constraints.[3] Wafer thickness repeatability is critical for process control, as the passive element device performance is impacted by change in its proximity to back metal ground planes. Therefore, a quick measurement system is required to ensure all wafers are within specifications for both the mechanical thinning and polishing steps.

A cassette to cassette measurement system has been utilized to increase stage throughput by approximately 40%. The implementation of this step was made difficult because this machine had never been converted to accommodate larger size wafers. Since the 100mm process utilized custom equipment hardware and software, similar changes were required to convert to the 150mm process before regular engineering intervention was eliminated. Automatically downloading data from the measurement tool into Datalog, the manufacturing software that calculates the amount of removal at both grind and polish etch, was implemented. This provides a fully automated process with a lot of time savings due to decreased operator intervention from data entry.

A few process modifications were needed to convert the mechanical thinning process. First, the amount of material removed during the mechanical thinning process was increased to compensate for the slower wet etch polishing step. Second, other process parameters needed to be changed to improve uniformity across a larger wafer surface. Finally, the hardest task to overcome in the mechanical thinning module was the implementation of the individual wafer process versus a batch thinning process. The individual wafer process would look at the original wafer thickness and determine how much material would need to be removed to hit a consistent target. This was achieved with the automatic download from the measurement tool to a server and back to the thinning tool. With this methodology, the wafer data could be stored until the thinning tool required it.

The wet polishing process required a lot of time and characterization. Research was done to choose an appropriate wet etch chemistry. Then further research and experimentation determined the proper ratio of components and length of time needed to remove all mechanical thinning surface damage. After the chemistry was installed in the spray acid tool, the proper rotation speed needed to obtain optimum uniformity was established. The etching of GaAs is typically a very exothermic process. Therefore, the initial process worked for a long time until both the lot sizes and the volume of material going through the area increased. At this point, it was concluded that the tool had a temperature control issue. A new chiller and temperature controllers were installed to keep the process in control no matter what the run rate was in the area. This issue emphasizes the concept and the need for volume learning.

Photo Patterning

The greatest challenge associated with the conversion was to develop a new photo resist thickness. The decreased selectivity for the dry etch required a thicker resist layer, which required new characterization. Additional cost was incurred to purchase specialized equipment for thick resist coating. Older style SVG coaters struggle with uniformity for the thicker resists. The need for redundancy and additional throughput has meant attempting to match photo processes on different equipment sets, which requires additional time in the 150mm conversion plan.

A common method to remove resist buildup on the outer edge of the mounted substrate is chemical edge bead removal. A known drawback to this approach is the swelling of the resist along the wafer perimeter. Both the 100mm and now the 150mm processes utilize an optical edge bead removal (OEBR) or an optical exclusion ring that is incorporated into the 1X backside via mask. This mask revision allows for a consistent edge bead. For the 150mm process, the solution edge bead was re-incorporated into the process, but this time, the solution is sprayed very close to the edge of the wafer. The mask provides a larger edge exclusion then solution edge bead while being more consistent. In this combination, the photoresist on the edge of the composite is removed in addition to allowing for the swelled photoresist to be removed during the develop process. The combination reduces the amount of particulates that could end up in the etch chamber and thus cause wafer cooling issues.

Via Etch

After the backside photo process is completed, the wafers are ready for the dry etch process. The dry etch process etches through the 1-4mils of Gallium Arsenide and selectively stops on gold.

Figure 2. Etch bay populated multi-chamber ICP etch tools.

There were three main issues with converting from 100mm to 150mm that needed to be resolved. As mentioned previously, a number of wafers had difficulty clamping to the electrostatic chuck due to more bow. This was resolved by decreasing the thermal stressing of the composite and increasing the ESC clamping force. Secondly, the process required re-characterization to adjust for increased exposure area. After the main process was determined, the breakthrough step was revised and a descum step was added. The row of etch tools is shown in Figure 2. These two steps greatly reduced any defects caused by macromasking. Lastly, the new process was found to be more sensitive to changes in exposed area so tighter controls on OBER and the etch process were implemented.

Demount of Wafer from Carrier

The final hurdle was capacity of the demount process. This process is where the 20-100µm thick wafer with thousands of vias is separated from the sapphire carrier. As in the 100mm process, the wafer is separated from the sapphire by dissolving the adhesive while gravity lets the wafer fall into a custom demount cell. Although the patented hands-free demount cells allow cassette to cassette processing through this stage, the cycle time increased due to only one 150mm cassette fitting per tank. There was also a 10% increase in time to fully dissolve the adhesive on 150mm wafers. The desire was to have a larger capacity and more automated batch demount process with no fractures and no chemical residues. A unique solution was needed. Therefore, a custom automated demount hood was installed and implemented allowing more than 2200 wafers per week capacity as shown in Figure 3.

Figure 3. High capacity automated demount hood for 150mm substrates

Though the installation of such a large automated hood had some issues, the grief was well worth the results. Cassettes of wafers are moved through four solvent baths. The first bath has been recycled while the last is freshly poured. This

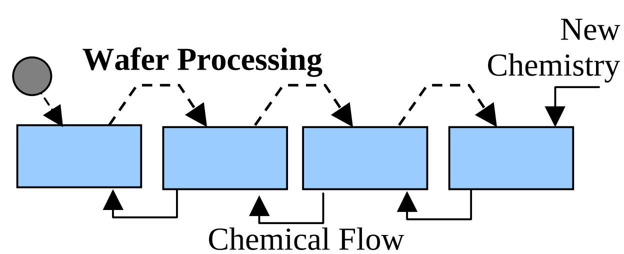

Figure 4: Flow of Wafers and Solvents for the Demount Process

recycling mechanism, shown in Figure 4, in combination with various temperature set points decreases both the possibility of residue and process time.

After being demounted, the wafers are automatically loaded into a dump rinse tank. Then the completed cassettes of wafers are dried in a separate spin rinse dryer with no harm to the wafer. Since the implementation of this automated hood, the process time has decreased almost to match process time for 100mm wafers. Operator intervention has also greatly decreased since moving from the manual process, which required agitation, to a fully automated process.

Lessons Learned

Most valuable lessons learned during the capacity ramp and wafer size conversion could be categorized into three areas: volume learning, proactive feasibility studies, and timing. The first lesson is that volume learning is necessary to forecast the potential pitfalls uncovered by high volume production. No amount of process characterization and testing by engineering can mimic day to day variation associated with manufacturing. Development of the manufacturing expertise to anticipate process issues and correct them before they happen takes time, and wafers.

Secondly, proactive feasibility studies allow the process engineer to determine the equipment and process feasibility early enough to make others aware of potential changes. The importance of timely evaluation/characterization using a 150mm verses 100mm substrate cannot be overemphasized. Subtle processing differences (i.e. carrier bow, ICP etch polymer formation, wet etch/cleans sensitivity to wafer rpms, etc.) can have a significant impact on process robustness. Maximizing of measurements and inspections in the early conversion phases can pay for themselves many times over by allowing timely process adjustments to be made in order to compensate for any wafer format size process effects.

Finally, the optimum timing of a wafer size conversion depends upon whom is asked. The financial analysts will not want to take on the conversion costs until the need *has* been justified and then expect it to contribute to additional sales virtually immediately without issue. The engineering team would like to invest during downtrends in the business such that more equipment and process characterization could be done to allow for a more successful ramp. Unfortunately, many business models ask that funding be cut back when the demand is low and only allow spending when a factory can't keep up.

A factory running at capacity requires exemplary uptime of equipment to allow for a subset to be converted to 150mm. Hopefully the process correlation between the two wafer sizes allows for a quick turn on so the 150mm tool can begin contributing to running product. In the case of the through substrate via process, some equipment was not convertible thus forcing the engineering teams to balance process changes, re-characterization, discovering 150mm limitations with 100mm tool sets, and attempting to run very high volume production. Within 3months of converting the through substrate via process line to 150mm, the line broke the 1000 wafer a week barrier again; this time at 150mm.

Conclusions

The through substrate via process faced a variety of challenges during the conversion to 150mm. Maintaining competitive wafer costs requires the minimization of resource costs largely attributed to people and mounting substrates, both of which increased for the 150mm process. Equipment limitations processing 150mm mounted wafers and greater process sensitivity created technical challenges that required significant attention. Establishing a low cost, high volume capable process required a balancing of these two constraints.

Additional costs and resources spent up front can save much more in the end by providing a higher yielding, lower cycle time, more cost efficient process. Equipment that may be thought to be process capable when converted to 150mm may not be, and can require long lead-time equipment purchases jeopardizing customer commitments. High volume through substrate interconnect processing equipment is becoming more available, but depending upon your process, there are likely many hurdles when converting to 150mm which only time, money, and talent can resolve.

Acknowledgments

The authors would like to thank Terry Daly, Christine Rummel, Hilton Fowler, Gabriel Hernandez, Adrienne Johnson, Alaina Barros, Kurt Pillote, Lup Yee, Dirk Bottesch and others who shared their technical and manufacturing contributions on through substrate vias. We would especially like to thank all the operators and technicians that were willing to provide feedback in order to make the source via process more manufacturable and a very successful endeavor.

References

[1] C. Varmazis, G. S. D'Urso, H. Hendriks, *Semiconductor International*, Dec. 2000

[2] R. Williams, Modern GaAs Processing Techniques, Artech House, Inc., Norwood, MA, 1990

[3] K. M. Adams, L. S. Klingbeil, *GaAs MANTECH 2000*, p.74-78.