

Manufacturing 6-inch GaAs substrates by the VB method

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Abstract

Manufacturing systems for producing 6-inch GaAs substrates are refined by optimizing the Vertical Boat (VB) method and the wafer polishing process. Introduction of low cost facilities leads to reduced manufacturing cost. The Taguchi method assists in the design of a furnace structure with a stable thermal environment and polishing conditions resulting in stable surface quality. New production facilities have been constructed while maintaining consistent quality.

INTRODUCTION

The shift to 6-inch manufacturing of GaAs devices has been driven by the need to reduce manufacturing costs. To realize the potential economy of scale that larger wafers provide, device manufacturers require the highest quality, most uniform wafers that can be manufactured at competitive costs. This paper describes Sumitomo Electric’s strategy for substrate production and discusses the production process from the perspective of cost effective manufacturing. The Taguchi method helps to refine the VB method for bulk crystal growth and wafer processing. Quality of 6-inch substrates is also discussed.

COST EFFECTIVE MANUFACTURING

1. STRATEGY FOR COST EFFECTIVE MANUFACTURING

Cost effective manufacturing has 2 aspects. One is the reduction of direct production cost by improving the process, such as yield improvement or increasing of lot size. The other is the reduction of indirect production cost by reducing investment cost, and introduction of new facilities with high productivity. The development of a 6-inch manufacturing process has been implemented considering both direct and indirect cost reduction.

Table 1 shows a comparison between the Liquid Encapsulated Czochralski (LEC) and VB methods. The quality of substrates is indicated as wafer breakage in handling, slip generation on the substrate surface in device processing, and dislocation density. The quality of substrates

TABLE 1
Comparison of 6-inch GaAs crystals by LEC and VB method

		LEC	VB	VB (2001)
Quality	Breakage, Slip	Poor	Good	Good
	EPD	Poor	Good	Good
	Ion implantation	Good	Good	Good
	Epitaxy	Good	Very Good	Very Good
Productivity	Lot size	Good	Med.	<u>GOOD</u>
	Furnace price	High	Low	Low
Production cost per unit area	Direct +	Low	Med.	<u>LOW</u>
	Indirect			

produced by the VB method is superior to those produced by LEC method [1,2], and the cost of VB furnaces is lower than the cost of LEC capital equipment. Fig.1 shows the facility cost per unit wafer area (4-inch and 6-inch by VB and LEC crystal in 1990).

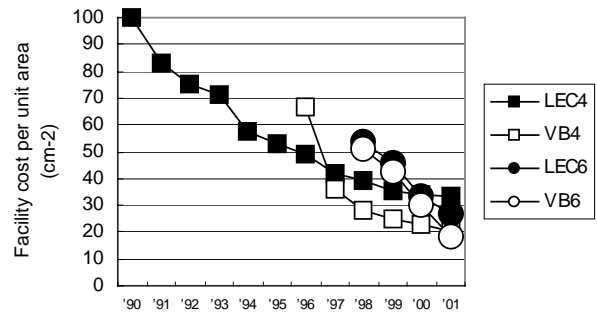


Fig.1 Facility cost per unit area by VB and LEC

We are reducing the furnace cost gradually through the simplification of the structure. In addition, productivity per furnace is gradually increasing through larger lot sizes and yield improvement. As the result, facility cost per unit area is showing improvement through time. However, the lot size of 6-inch crystal produced by the VB method was small, so that the facility cost per unit area had only a small advantage relative to the LEC method. We therefore focused on the improvement of lot size, and succeeded in the development of a long VB grown GaAs single crystal ingot. This was

effective for the reduction of indirect cost and better total cost performance in comparison with LEC.

Fig.2 shows the trend of the process cost per unit wafer area for polishing wafers, including both direct and indirect cost. The numbers are normalized to 4-inch total processing cost in 1990. In 1991, leading the way among compound semiconductor wafer manufacturers, we introduced the technology of 4-inch full-automatic multi-wafer polishing line (HYPER LINE). Processing cost was drastically reduced in 1991. After that, the process cost decreased gradually through the reduction of machinery cost and the improvement of yield. With the introduction of the 6-inch substrates processing line, however, we needed to re-consider our process strategy to determine the most effective method.

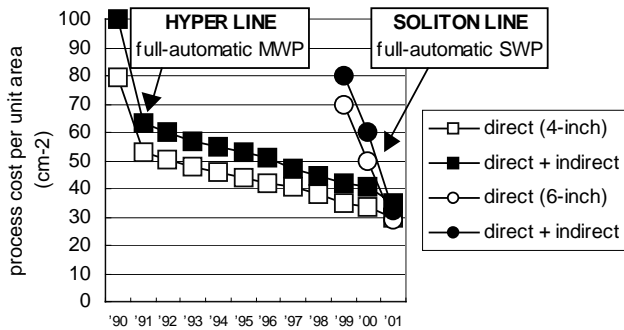


Fig.2 Process cost per unit area

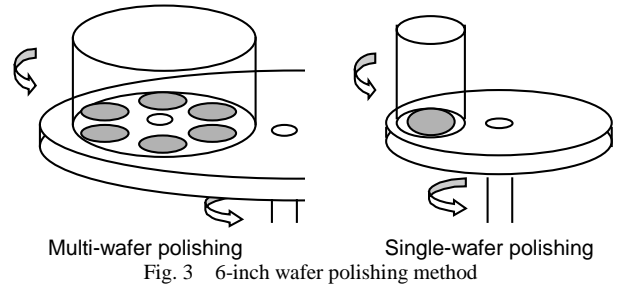
Table 2 and Fig.3 show a comparison of multi-wafer polishing (MWP) and single-wafer polishing (SWP). Both methods have similar performance in surface flatness. MWP has the advantage of polishing many wafers at the same time. However, the larger size of 6-inch substrates creates a problem. The large plates and automatic machines needed to transfer these plates occupy a large area in clean room. Clean room space is expensive, and the high cost of the necessary machinery increase indirect cost. In our estimation, the process cost for MWP is higher than that of SWP. Based on this, we selected full-automatic SWP line (SOLITON LINE) to reduce equipment cost for polishing of 6-inch substrates.

TABLE 2 Comparison of polishing process

		MWP 4-inch	MWP 6-inch	SWP 6-inch
Quality	Flatness	Good	Good	Good
	Surface cleanliness	Good	Good	Good
Productivity	Batch size	6 - 12	3 - 8	1
	Machine price	4 - 8	5 - 10	I
	Occupied area	8	10	I
Processing cost	Direct + Indirect	Low	Med.	Low

2.THE DEVELOPMENT OF LARGE SIZE INGOT

The development of long 6-inch GaAs crystal requires an optimized thermal environment. It is necessary to control liquid-solid interface shape in order to prevent the formation of polycrystal and keep a stable thermal environment. We focus on the furnace structure which effects the thermal environment as shown in Fig.4. Several structure parameters such as pedestal shape and materials with different thermal conductivity are chosen to simulate the



change in temperature profile from the beginning of crystal

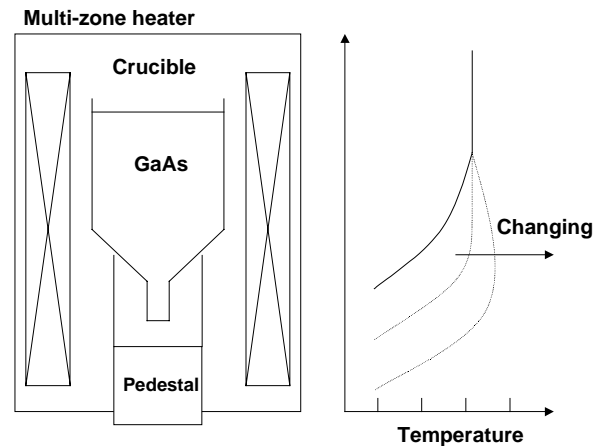


Fig. 4 Furnace structure of VB method and temperature profile.

growth to the end . The computer simulation of temperature distribution is made by the fine element method using FIDAP [3].

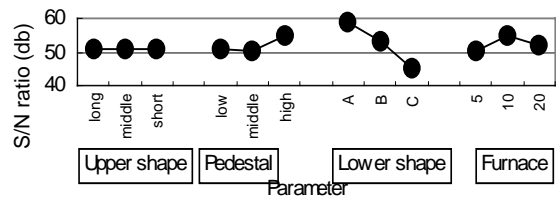


Fig.5 The cause and effect diagram (Temperature variation)

The Taguchi method is used to isolate parameters which strongly effect the variation of the thermal environment changing parameters based on the orthogonal array, the effect of each parameter on the variation of the thermal environment through the crystal growth is evaluated. Fig.5 is the cause and effect diagram which shows the effectiveness of the parameter changes on the thermal environment. A larger S/N ratio indicates less variation in the temperature profile. We selected a furnace structure which seems to

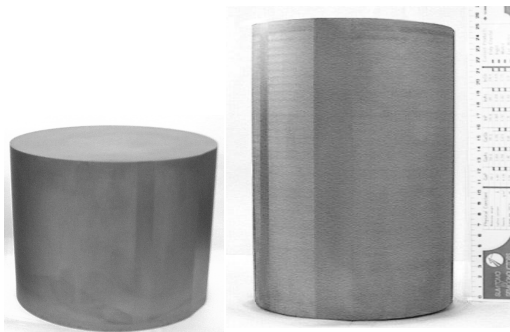
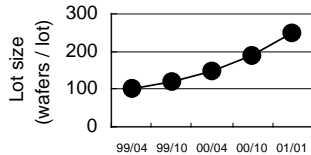


Fig.6 The development of 6-inch GaAs lot size

reduce variation of temperature. The optimized structure selected through use of the Taguchi method has led to the development of long 6-inch crystals as shown in Fig. 6.

3.THE DEVELOPMENT OF SINGLE-WAFER-POLISHING

Substrates users pay close attention to wafer surface quality. In wafer polishing, the flatness and cleanliness are the most important factors. Previously, SWP was considered to

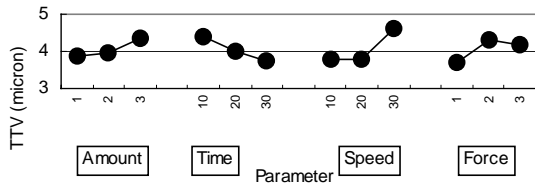


Fig.7 The cause and effect diagram (TTV)

have a problem with wafer to wafer variation. The Taguchi method was also used to optimize the polishing condition for good flatness and wafer to wafer variation of flatness. Parameters for several conditions are presented in an orthogonal array. Following a combination of process conditions, we made a trial examination of polishing. We evaluated each wafer flatness and wafer to wafer variation of flatness. The cause and effect diagram shown in Fig7

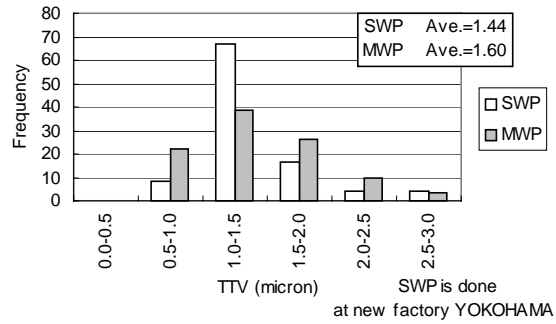


Fig.8 TTV histogram for MWP and SWP

indicates the parameter effectiveness for TTV. By optimizing the process conditions, we have developed the surface condition which are substantially similar to the quality produced by MWP. Fig.8 shows the comparison of 6-inch TTV between MWP and SWP. By selecting a SWP method, the total cost of 6-inch GaAs substrate processing can be minimized for large scale production.

6-INCH SUBSTRATES QUALITY

The Taguchi method is an effective guide for stable supply with high and uniform quality. The crystal defect (EPD of molten KOH) is generated from thermal stress. The

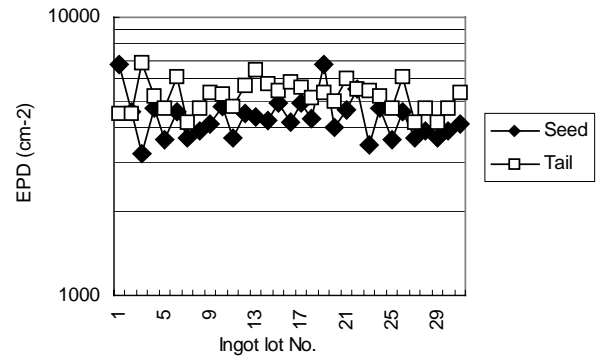


Fig.9 Ingot lot to lot variation of EPD (6-inch)

stable thermal environment controls the crystal growth with stable thermal stress environment. Fig.9 shows data for the variation of quality from lot to lot. 6-inch substrates by the VB method are controlled with good repeatability of EPD from 2000 to 7000 cm-2.

The microscopic property of substrates by VB method is investigated. Fig.10 shows the resistivity profiles, measured at 100 micron pitches from center to the periphery. LEC crystals need multi-step annealing to have good uniformity of microscopic resistivity[4]. It leads to high production cost and generation of residual strain due to high temperature annealing. VB crystals, however, have the highest

homogeneity of microscopic resistivity only by 1-step annealing, due to low crystal defects.

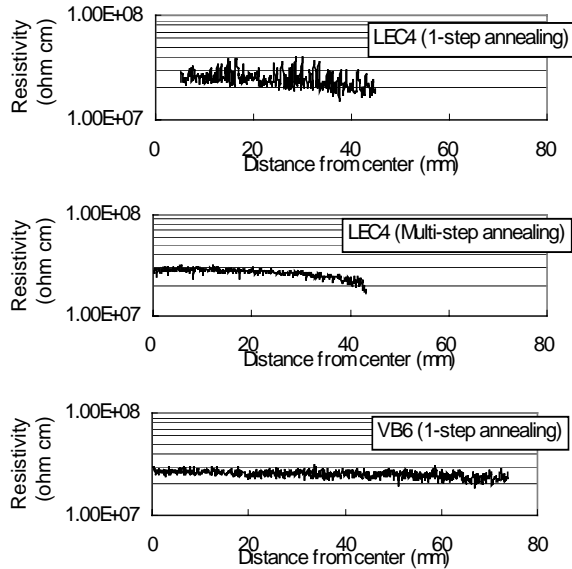


Fig.10 The uniformity of resistivity

We have also analyzed the property of ion-implanted layers on 6-inch VB substrates. ²⁹Silicon + ions were implanted into VB and LEC substrates through Si₃N₄ at the energy of 90keV with a dosage of $3.0 \times 10^{12} \text{cm}^{-2}$. The sheet resistance of I₂ layers was measured after rapid thermal annealing. The relationship between the resistivity in the substrates and the sheet resistance of the ion-implanted layer are shown in Fig.11. Sheet resistance of 6-inch VB substrate shows the same dependence on substrates resistivity as 4-inch LEC and 4-inch VB substrates.

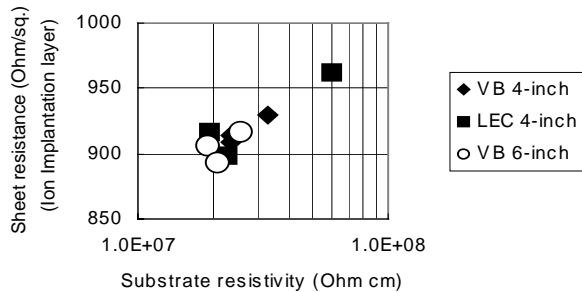


Fig.11 Sheet resistance of I₂ layer

Fig.12 shows the V_{th} variation of ingot to ingot and batch to batch FET process. It was reported previously that the substrates grown by the Vertical Gradient Freeze (VGF)

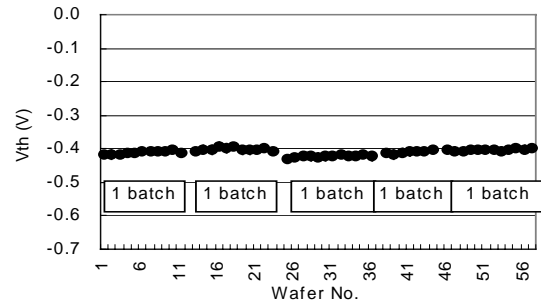


Fig.12 The variation of device property

method had high variation of V_{th} [5]. However, devices made from VB crystals show good reproducibility.

The properties of epitaxial layers on 6-inch VB substrates were also evaluated. Our internal OMVPE group is producing highly uniform 6-inch epitaxial wafers, comparable to 4-inch epitaxial wafers. Fig.13 shows an example. A capless double delta doped P-HEMT structure was fabricated with a sheet resistance variation less than 1%. This shows a uniformity similar to that of 4-inch epitaxial wafers.

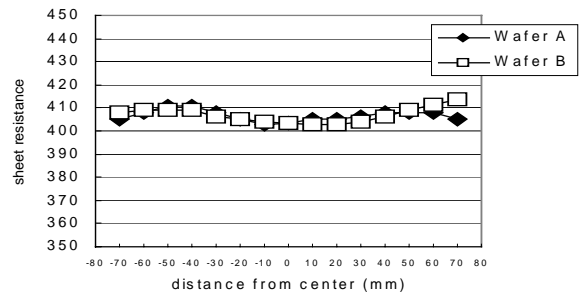


Fig.13(a) The uniformity of sheet resistance measured by LEHIGHTON

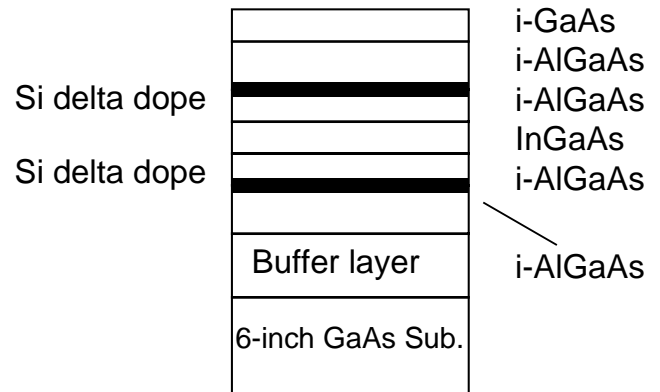


Fig.13(b) Capless double delta doped P-HEMT structure

THE EXPANSION OF PRODUCTION SITES

We have invested in new compound semiconductor manufacturing facilities in Japan, Taiwan and the United States. These new facilities are located near our customer base and will allow us to react quickly to their needs for production and technical development. Moreover, our investment leads to another advantage. We can guarantee the stable supply, avoiding the risks such as the earthquake or accidents. However, a geographically diverse production base can lead to variation of quality between facilities. To minimize this possible variation, our production lines are optimized using newly introduced quality engineering techniques such as the Taguchi method in addition to the quality control systems that have long been used in Sumitomo Electric's manufacturing. Fig.14 shows the surface cleanness of wafers produced in Itami (MWP) and Yokohama facilities (SWP). The data show no difference between production sites in surface quality.

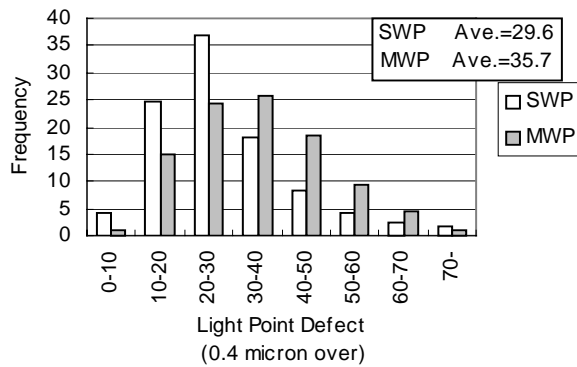


Fig.14 Surface property at ITAMI and YOKOHAMA factory

SUMMARY

The market requires mass production of 6-inch GaAs substrates with high quality and low price. To respond to this market requirement, we focus on the cost effective manufacturing by reduction of direct production cost and indirect investment cost. The optimization of crystal growth furnaces, the introduction of single-wafer-polishing process, and the establishment of new facilities make it possible to respond to market requirements effectively.

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