Recycling Processed GaAs Wafers

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Abstract

Over the last several years, we have developed processes for strip-back and re-polish of process-monitor wafers as well as scrapped GaAs wafers from all points in the various TriQuint fabrication flows. Initial efforts produced several thousand mechanical grade wafers with high yields. Current processes produce prime wafers that meet all the TriQuint GaAs substrate specification criteria. These have been shown in initial production fabrication run trials to work generally as well as virgin GaAs wafers. The obstacles overcome in this development will be discussed and production lot electrical data will be presented to demonstrate the value of this promising and frugal workaround to the current worldwide wafer shortage.

1. Introduction

Thrift, thrift, Horatio! the funeral baked meats

Did coldly furnish forth the marriage tables.

Hamlet, Act i. Sc. 2

Unlike the thrift Hamlet disparages above, reuse of GaAs process monitor/control wafers and of scrapped production wafers makes good sense. This is especially true in today's climate of scarce and expensive wafers and high raw material cost.

At TriQuint, those wafers are first available "as is" for process engineering use. In the past, when that use was exhausted, the wafers were collected and discarded. As foreign as the idea is with today's very high Ga and As costs, that material had to be disposed of as toxic waste at no small expense. This was a gross waste of perfect single crystal GaAs wafers often only used for a single blanket implant or other process qualification.

Since 1997 we have been collecting such wafers to recycle at PicoPolish for GaAs mechanical wafers. We began with non-metallized wafers, but now can do intact wafers scrapped anywhere in our fabrication processes. From use only as mechanical wafers, we branched into use of re-polished wafers as implant control wafers with good results. This led to the current investigations, which focus on re-cycling wafers into complete conformance with our substrate specifications for production use.

2. Techniques for re-polish

Prior to polishing, layers have to be removed from the semiconductor surface. This operation, called "strip and etch," is done by dipping the wafers into successive baths. Then, wafers are rinsed, dried, and visually controlled. Following layer removal, wafers present patterns (see Fig. 1A). Techniques for re-polish mainly depend on the remaining patterns and on customer specifications.

Generally, polishing GaAs wafers is done in 2 steps: one for stock removal (see Fig. 1B) and the second to reduce microroughness (haze) and particle contamination (see Fig. 1C). Wafers are mounted on carriers using templates. The template material is chosen in consideration of the process.

During the stock removal step, we control the removal rate, and the total thickness variation (TTV). We adjust the length of this step considering the remaining patterns. After this step, the wafer surfaces are slightly rough and hydrophilic but are free of scratches.

The second and final step reduces roughness and particle contamination. We use a softer polishing pad here to obtain a mirror-like surface.

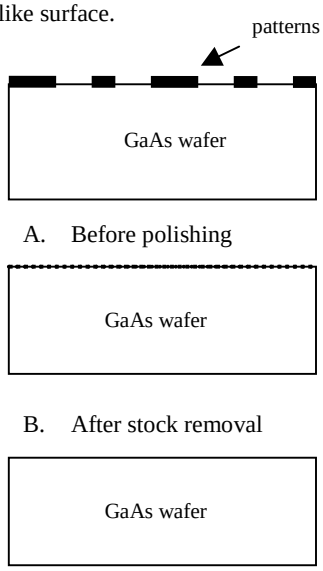

Fig. 1 Schematic representation of GaAs wafer polishing sequence

3. Mechanical properties

The challenges for re-polishing are (1) to achieve particle specifications without damaging mechanical parameters and with a good yield (80-90%) (2) to have minimal thickness removal in order to reclaim wafers several times and (3) to minimize final TTV for standard microelectronic process uses.

Wafer mechanical parameters are measured on non-contact equipment. Our latest improvements lead to a TTV damage of only 2.2 µm for the whole polishing sequence. We remove 10 µm maximum for most patterned wafers. Average removed thickness in the final polishing is 3 µm, and TTV deterioration

is less than 0.5 µm. After final polishing, wafers are cleaned in specific baths. These processes have been developed enough for re-polished wafers to meet prime wafer specifications, allowing production use of reclaimed wafers.

Work to date has been primarily on 100 mm wafers, but we have recently obtained similar results with 150 mm wafers: average TTV of 5 microns, minimal thickness removed, and surface preparation for production processing.

Table 1 below shows final mechanical results on a whole batch. TTV values include TTV before polishing, which is never null.

	Sampling		50
	Center Thickness	TTV	TIR
	(µm)	(µm)	(µm)
Min	600,31	2,37	2,27
Max	621,45	12,50	9,71
Average	611,42	5,40	4,56
Range	21,14	10,13	7,44
Std Dev.	6,64	1,94	1,55

Table 1 Final mechanical parameters after polishing for 100 mm diameter reclaimed GaAs wafers

Concerning particle contamination, LPD (Light Point Defect) measurements are performed with a Surfscan 5500. For mechanical grade, wafers are scanned down to a particle size of 0.38 µm. Current performance is 0-50 particles > 0,38 µm (see Fig. 2). For prime quality, we control down to 0.23 µm to assure a better and a more stable final polishing step. For improvements on LPDs, we can measure some engineering wafers on a Surfscan SP1, allowing more accurate measurements.

In addition, "defect area" represents the total amount of scratches or big defects on the surface and is a good indicator for the quality of polishing. We currently obtain defect areas of less than 1 mm^2 for 100 mm wafers.

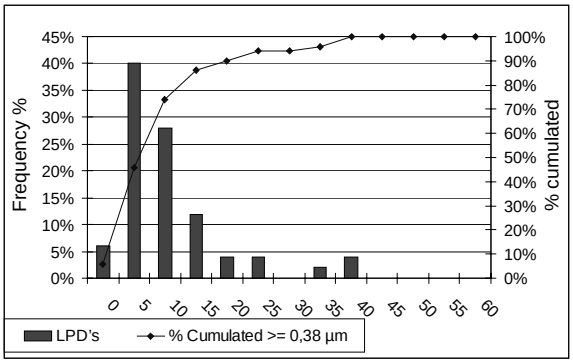

Fig. 2 LPD's frequency and cumulative LPD's at 0.38 µm (Surfscan 5500)

Finally, we have measured metallic contamination by Total Reflectance X-Ray Fluorescence (TXRF) on 100 mm GaAs wafers. Results have shown no metallic contamination such as gold or titanium peaks in the TXRF spectra due to strip and/or etch residues.

4. Production Results

TriQuint substrate specifications are intentionally kept as simple as possible to avoid higher than necessary wafer cost. All specified parameters are believed important to successful use in fabrication and specification limits are made no tighter than we believe are needed to maintain fab yields.

Once re-cycled wafers meeting prime wafer specifications were available, they could be tried in production processes. Since the wafers we recycled originally conformed to TriQuint electrical specification, re-polish could focus on meeting mechanical (flatness) specifications. This was verified when initial success was obtained on blanket implant tests on re-polished wafers (most of which were previously implanted and annealed). No re-measurements of resistivity or mobility were done after re-polish.

For seamless integration into automated high-volume production processing, the question of laser marks had to be addressed. The vendor-supplied laser mark is the only identification on wafers going through the TriQuint fab line. It is read multiple times by operators, and by Optical Character Recognition (OCR) systems on fab tools, and is used to sort wafers and to look up production parameters like mask set, test plan, etc.

In most cases, the original laser mark was deep enough to survive re-polishing. Then, we had only to alter the original laser mark in our wafer database to prevent look-ups from finding the original fab run rather than the current one. In cases where the original mark is removed by re-polishing, a new laser mark will need to be written on the wafers, but we have not yet used that option in the early trials described here.

The first test of re-polished wafers was naturally done in a process with broad spec latitude. This process features a single power FET nominally shutting off (pinchoff voltage Vp to 1 uA/um) at –2.3 V but with a very broad Vp window of 800 mV. The results of that first test are shown in Fig. 3.

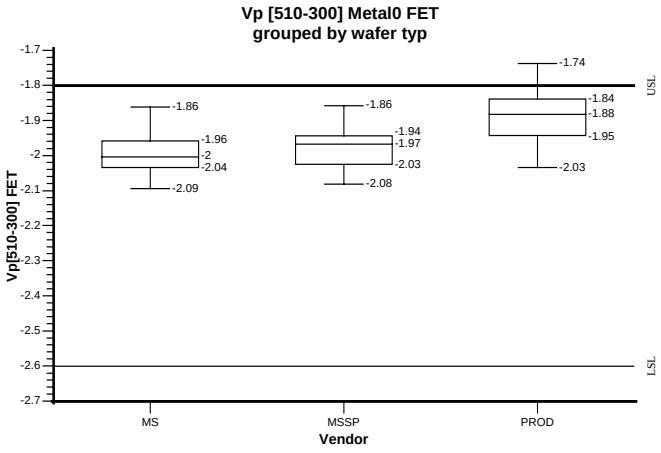

Fig. 3. Quartile plots of standard material and two re-polish variants

In the figure, the first two ranges are two re-polish variants (5 wafers each) and the final range is the 15 standard wafers which comprised the rest of the run. In this run, the standard wafers were off center positive in the Vp specification, while the re-polished wafers were also positive in Vp, but not as much. No difference was seen between the two re-polish types.

After completion of fab, the wafers in this first run were die-sorted. As expected from their closer to nominal pinchoff voltages, the re-polished wafers gave better sort results than the standard wafers.

Having seen encouraging results in our initial tests, further tests were launched on larger quantities of re-polished wafers used in that same process and in several other processes with tighter specification windows and multiple implants and FET types.

Fig. 4 shows the sheet resistance results for two implants ("D" and "G") for two process runs in different flows. In each case, the wafers shown first are the standard wafers (from one or more different vendors) and those shown second are the re-polished wafers. The order of wafers in fab was randomized several times during the process to avoid confusing wafer effects with any transient "down the run" effects.

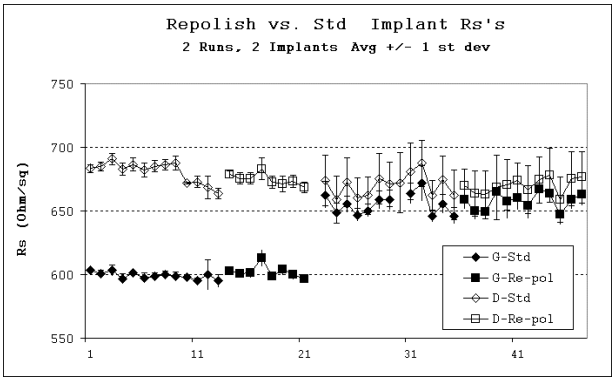

Fig. 4 Sheet Resistances

The figure shows that the sheet resistances of all wafers is very similar. Nothing stands out on the re-polished wafers. One of the runs had anomalously variable sheet resistances, but that was also reflected in both standard and re-polished wafers.

The same is true for the pinchoff voltages of the Depletion (D) FET and the Power (G) FET, as shown in Figs. 5 and 6. Again, parametrically the re-polished wafers look indistinguishable from the standard wafers. Indeed, in some cases the re-polished wafers seem to show more uniform on-wafer Vp. This could be related to the fact that re-polished wafers would usually already have been rapid thermal annealed (RTA), and would thus have already undergone any wafer distortion that can sometimes lead to alignment difficulties from before to after RTA.

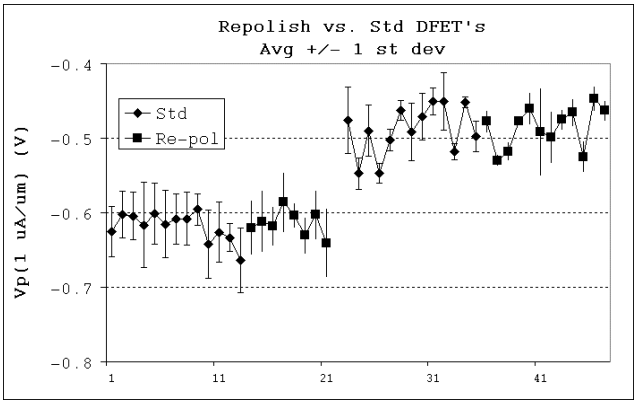

Fig. 5 Depletion Mode FET Pinchoff Voltage Results

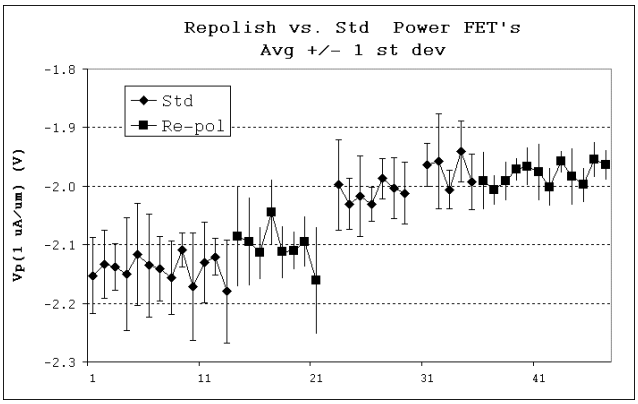

Fig. 6 Pwer FET Pinchoff Voltage Results

6. Conclusions

We have demonstrated in early trials that re-polished wafers which meet prime wafer substrate specifications can be used in production runs without noticeable effect on parametric test results or device yields. Continuing verification of this using very large quantities of wafers will be done to verify the lack of any subtle or small effects.