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A Very High Performance, High Yield, and High Throughput Millimeter Wave Power pHEMT Process Technology

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Abstract

A high performance, high yield, and high throughput millimeter-wave, Q band, power pHEMT process technology has been developed. It utilizes double recess, selective etch, optimized expitaxial layer structure, individually grounded source via holes, and a hybrid Tee-gate. Linear power amplifiers (37-40 GHZ) with small signal gain of 18±1 dB, saturated output power of 30.5 dBm, DC yield >50%, and RF Yield ~100% are being shipped in commercial quantities. Q bands power amplifiers (43.5-45.5 GHZ) with average output power, across the band, of ~2 W, small signal gain of 18 dB, and power added efficiency of >22% are produced for internal use. The dependence of yield and RF performance on process parameters is discussed.

INTRODUCTION

AlGaAs/InGaAs power pHEMT is, at present, the device of choice for millimeter-wave power amplifiers [1-2]. The main process components/parameters that contribute to both performance and yield of these devices are: epitaxial layer structure, first recess width and current, gate lithography, and individually grounded backside source vias (ISV). There are often tradeoffs between yield, performance, and reliability.

In this paper, we discuss the dependence of device yield and performance on the aforementioned process parameters. Amplifier results for two representative circuits will be presented.

EPITAXIAL LAYER STRUCTURE AND ETCH STOP

A schematic cross sectional view of a generic pHEMT epitaxila layer structure is shown in Figure 1. The main features of this structure are: InGaAs channel with high Indium concentration (18-20%), double pulsed doping with a front to back pulse ration of 2-5, and an etch stop layer, not shown in the figure, for selective etching of the first recess. The etch stop layer can be either AlAs or AlGaAs. We have used a citric acid based wet etch for selectively etching GaAs. Selective First Recess, SFR, is vital to the fabrication of devices with consistent DC and RF parameters. Typical DC parameters for our devices are given in Table 1. If the gate recess is done non-selectively, the epitaxial layer structure should be designed such that it results in a gate recess depth of ≤ 300 Å. It must be noted that for high performance pHEMT devices, the threshold voltage has a sensitivity of 8-9 mV/ Å.

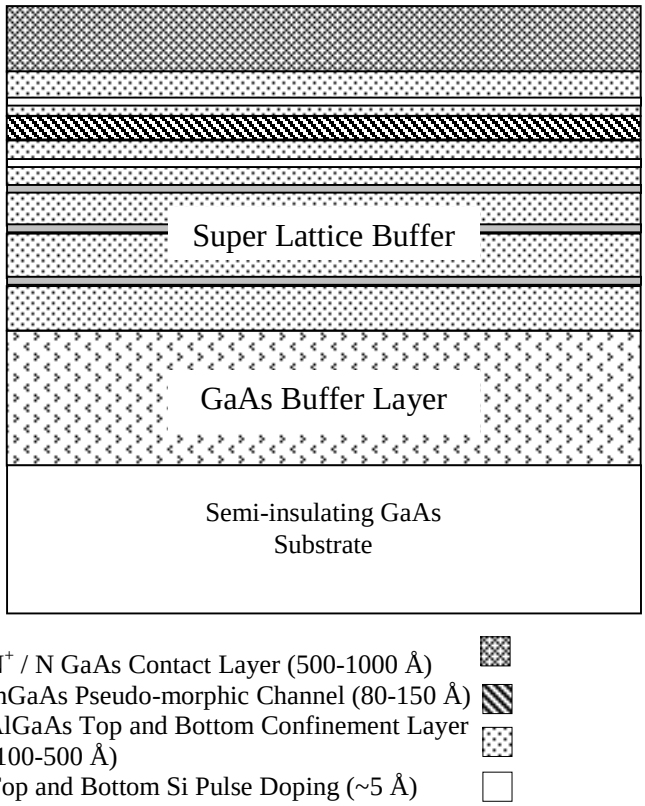

Figure 1. Generic power pHEMT epitaxial layer structure.

TABLE 1
Median Values of DC Device Parameters Measured on a Single Finger 100 μm Wide FET

Parameter	Symbol	Value	Unit
Maximum Drain Current	Imax	690	mA/mm
Drain Current at Vgs=0 V	Idss	260	mA/mm
Pinchoff	Vp	-0.73	V
Peak Transconductance	Gmp	517	mS/mm
Breakdown Voltage	BVdg1	11.6	V

FIRST RECESS CURRENT AND WIDTH

Both first recess current and width are very important parameters for determining the device performance at millimeter wave. In general, the first recess current should be chosen such that it does not impose a restriction, bottleneck, to the maximum drain current achievable by the intrinsic device. Two high a first recess current will severely limit the breakdown voltage and device reliability.

The first recess width should be made as small as possible subject to maintaining a sufficiently high breakdown voltage and acceptable DC yield. For the same RF performance in terms of power, gain, and efficiency, it is possible to obtain the same results if one simultaneously increase the first recess current and first recess width. This method also increases the alignment budget between the gate and first recesses, which translates into significant increase in both DC and RF yield. One has to be very careful not to increase the first recess current to such a high level that hot electron/hole effects become significant. Too much of hot electrons/holes generation makes the device susceptible to long term RF life power degradation. Figure 2 shows the tradeoffs between the first recess dimension first recess current and output power. All numbers are referenced to their nominal values. We have also experimentally observed that as long as the first recess current and width are chosen properly, the physical gate length, at the interface of Ti with AlGaAs Schottky layer, can be varied from 0.15 μm to 0.25 μm with no impact on the output power and very little impact on the small signal gain.

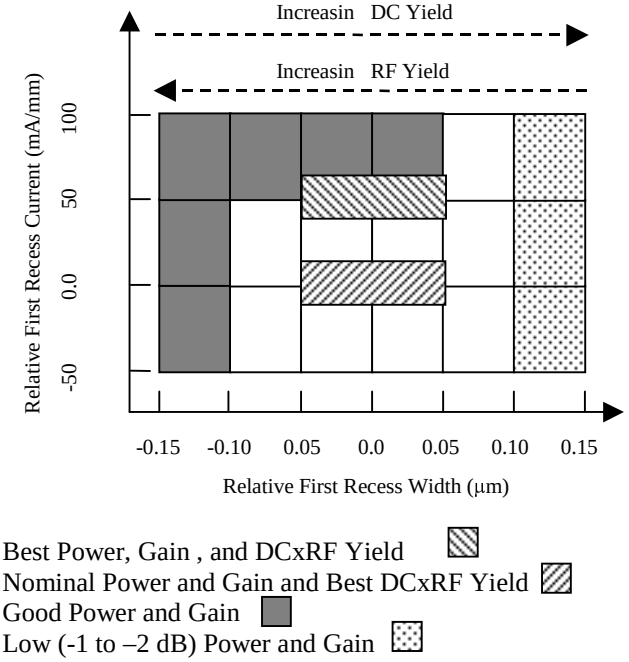

Figure 2. Performance dependence on first recess current and first recess width.

HYBRID TEE-GATE

Electron beam lithography, E-Beam, in combination with a PMMA/PMMA-PMAA/PMMA tri-layer resist has been traditionally used for fabrication of Tee-gates. It is also possible to use a bi-layer PMMA/PMMA-PMAA resist system. In this method, the exposure conditions of the copolymer (PMMA-PMAA) strongly impact the stem dimension defined in the bottom PMMA stem. Furthermore, the process depends on the differential developing rate of copolymer and PMMA for the formation of Tee-gate. This makes the stem dimension very sensitive to develop time, the thickness of the copolymer, and the consistency of the copolymer resist chemistry. Ideally, one would like to have a process in which the stem lithography can be done completely independent of the Tee-top formation. In this way, one would have 100% independent control over the shape and dimension of the stem and Tee-top (Cap) of a Tee-gate.

In hybrid Tee-gate process, the Tee-gate stem is written in just a single layer of PMMA. The Tee-top is formed using an I-line optical resist and an I-line stepper with a throughput of >30 wafers/hour. The control over the stem dimension is 8 times tighter than what is achievable in a tri-layer of bi-layer E-Beam resist processes. The wafer write time for the stem is 30 minutes per wafer in a shaped E-Beam machine as compared to >4 hours for a tri-layer process. Proper processing conditions minimizes or eliminates any interaction between the PMMA and the I-line Tee-top resist. Cross sectional view of a Ti/Pt/Au hybrid Tee-gate is shown in Figure 3.

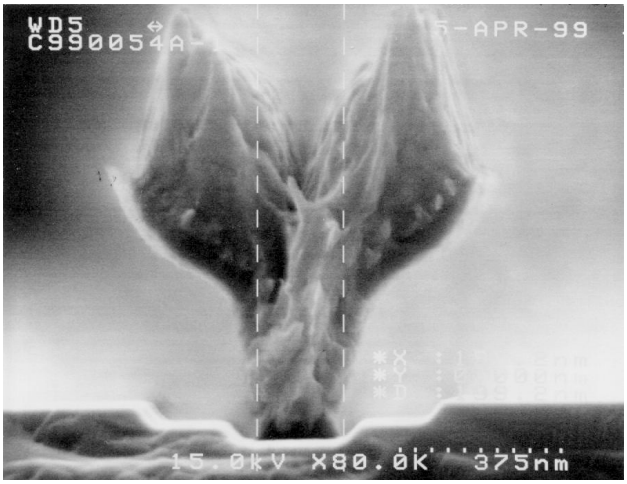

Figure 3. SEM cross section of a Hybrid Tee-gate. The gate metal is Ti/Pt/Au and gate is formed through liftoff.

INDIVIDUALLY GROUNDED SOURCE VIA (IGSV)

Good performance at millimeter waves requires minimization of the source inductance. This is achieved through grounding source of each individually FET. Backside contact to each individual source is accomplished through metallization of backside via holes in a 50 μm thick wafer. Drawbacks of this technique are increased processing cost and necessity for accurate control of the wafer thickness to ±5 μm. Although it is possible to make millimeter wave amplifiers without individually grounded source vias (IGSV), it would be difficult to achieve the same power and gain performance as that of IGSV technique used in this work.

AMPLIFIER RESULTS

Small signal gain for a typical three-stage Q band power amplifier is shown in Figure 4. The unit gate width for all FETs is 60 μm. The total periphery for the first, second, and third stages are 1.44 μm, 2.88 mm, and 3.84 mm. The total chip periphery is 8.16 mm. Gain vs. frequency characteristics for eight chips is shown in the figure. The bias conditions are: Vds=5 V and Id=1400 mA. Average power added efficiency is 25%. Peak power added efficiency is ~27%. Average DC yield for a six-month period of July 2000 to January 2001 is 57%. Maximum DC yield of 80% has been observed. Average RF yields is 94% for the same period.

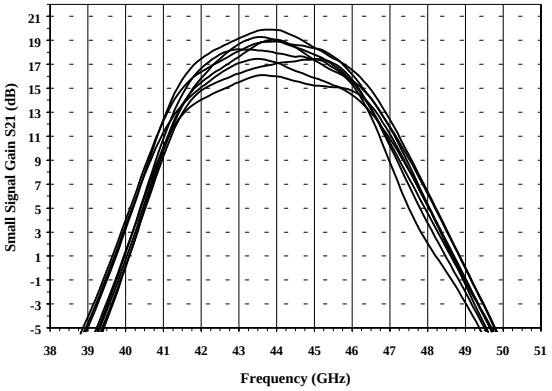

Figure 4. Small signal gain of a three-stage Q band power amplifier. For an input power of 19 dBm and over the 43.5-45.5 GHz band, the average output power, in dBm, for the eight chips shown is: 32.54, 32.55, 32.63, 32.87, 32.68, 31.71, 32.71, and 32.65. See text for circuit details.

Figure 5 shows performance for a three-stage amplifier chip that has been shipped in commercial quantities for LMDS application. Average DC yield for a six-month period of July 2000 to January 2001 is 50%. Maximum DC yield of 87% has been observed. Average RF yields is 88% for the same period.

CONCLUSIONS

The major process parameters that influence the performance and yield of AlGaAs/InGaAs power pHEMT amplifiers for millimeter wave applications have been studied in details. A very high performance, high yield, and high throughput process has been developed through optimization of the epitaxial layer structure, first recess width, first recess current, a two-step hybrid Tee-gate lithography method, and individually grounded source via holes. Further increase in throughput should be obtained by using an all-optical lithography method for Tee-gate formation.

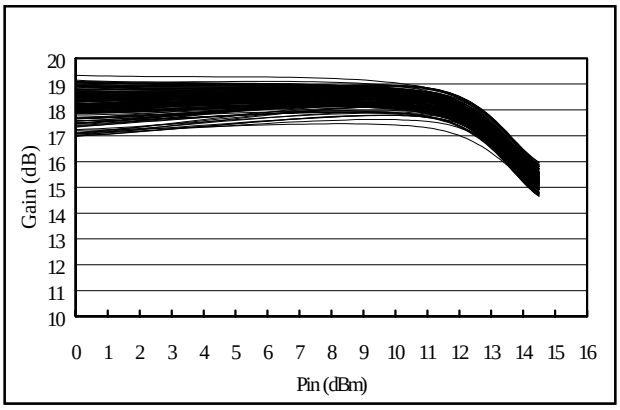

Figure 5. Gain vs. input power, Pin, characteristics for a commercial three-stage millimeter wave power amplifier at 39 GHz. Curves for 148 circuits are shown.

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