A Single Threshold Double Recessed pHEMT Process for Economical Fabrication of High Performance Power Amplifiers and Low Noise Amplifiers at X-Band

K. Alavi, B. Rizzi†, Dain Miller‡, S. Ogut, A. Bertrand, K. Kessler, F. Fay, C. Laighton, A. Bielunis

Raytheon RF Components Company
362 Lowell Street, Andover, Massachusetts, 01810, USA
Phone: 978.684.8598, e-mail: Kamal_Alavi@RRFC.Raytheon.com
† Tyco-electronics, MA/COM Lowell, ‡ Tyco-electronics, MA/COM Roanoke

Abstract

The integration of power and low noise amplifiers on a single chip offers the opportunity to achieve low T/R module cost through reduction in module size and decrease of MMIC die count. A 0.25 μm Tee-gate, double recessed InGaAs/AlGaAs pHEMT process with excellent power and low noise performance has been developed. Both high power and low noise amplifier MMIC circuits have been fabricated using this process. The measured performance is presented and the impact of the epitaxial layer structure and device geometry upon circuit performance is discussed.

INTRODUCTION

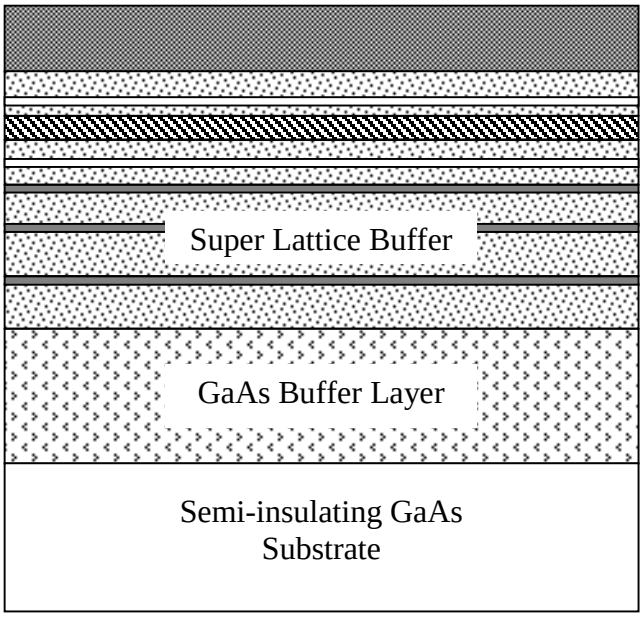
The Transmit/Receive modules continue to be inserted in numerous systems. It is highly desirable to increase the module performance and reduce cost simultaneously. Module cost can be reduced by decreasing the number of chips in a module, i.e., through higher level of integration as long as performance is not compromised. All functions, with the exception of the low-noise front end and the high power output amplifier, can be built successfully with a depletion mode MESFET or pHEMT process. This makes it possible to have high-performance three-chip modules consisting of pHEMT LNA chips, MESFET multifunction chips, and pHEMT PA chips [1-2]. Integration of PA and LNA functions in a single chip further reduces the module cons.

Traditionally, MESFET devices have been optimized either for low noise application or for power application. The unique expitaxial layer structure of a pHEMT device provides a great deal of freedom for device design.

In this work, five different epitaxial layer structures have been used for device fabrication in order to find the optimum structure for monolithic integration of both LNA and PA. RF measurement results are presented for discrete devices as well as MMICs at X-band.

EPITAXIAL LAYER AND DEVICE GEOMETRY

A schematic cross sectional view of a generic pHEMT epitaxila layer structure is shown in Figure 1. The two main material-related parameters investigated in this work are the channel sheet charge (Ns) and InGaAs channel Indium Content (In%). Table 1 shows the expitaxial layer structures used in our study. Different structures have In% varying from 16% to 20%, and channel thickness of 90-130 Å, and sheet charge of 1.8-3.5x10^{12} cm^{-2}. Both single recessed and double recessed devices have been investigated.



N^+ / N GaAs Contact Layer (500-1000 Å)
InGaAs Pseudo-morphic Channel (80-150 Å)
AlGaAs Top and Bottom Confinement Layer (100-500 Å)
Top and Bottom Si Pulse Doping (~5 Å)

Figure 1. Generic power pHEMT epitaxial layer structure.

A schematic cross section of a double recessed pHEMT device is shown in Figure 2. The variables I_1 and Imax are the first recess current and maximum current of the device, respectively.

TABLE 1
Epitaxial layers case numbers and structure types
All devices have double recess

Case Number	Material Type	Gate Length (μm)
1	Millimeter Wave, High Imax ,Type 1	0.25
2	Medium Imax, High In%, Type 2	0.25
4	Standard Low Noise Type 4	0.25
5	Standard Low Noise Type 4	0.15
6	Standard Power Type 5	0.25

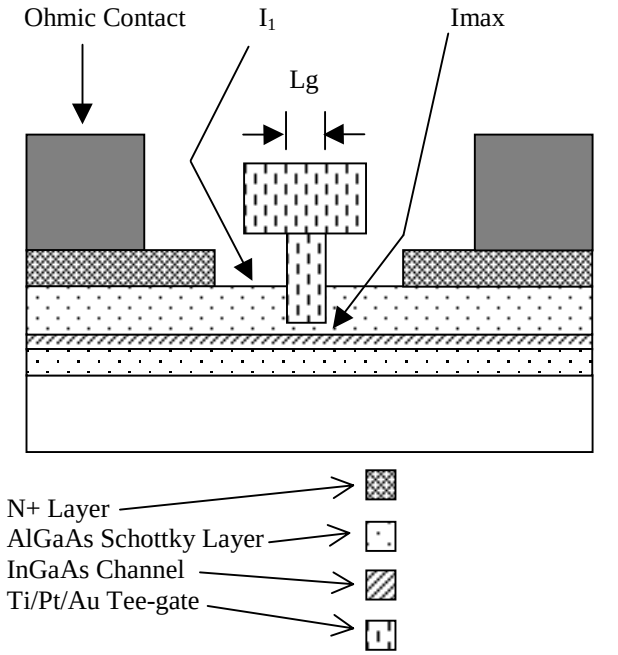


Figure 2. Schematic cross sectional view of a double recessed Tee-gate pHEMT process.

DISCERET DEVICE RESULTS

To characterize devices for low noise application, we have performed automated source pull measurements to determine the minimum noise figure and associated gain as a function of frequency at a standard bias point. For power characterization, devices were assembled in jigs with tunable input and output matching networks, which are then tuned by sliding conductive pucks while the device is under RF drive in order to obtain the optimum performance. In this study, both output power and power-added efficiency have been considered, attempting to obtain the best efficiency without significantly compromising output power.

Table 2 shows minimum niose figure, Fmin, and associated gain, Ga, at 8GHz, where experimental data from a number of devices of each type is presented. Although there is some spread in the noise figure data, there is no significant difference in minimum noise figure between any of the experimental devices. The device with reduced gate length (Case 5) has somewhat better noise figure. The higher Indium content material devices (Cases 1,2) do show higher gain, but do not show improved noise figure. The standard power device (Case 6) has lower gain than the double recessed low noise device (Case 4), but its gain of 12.5 dB is still quite reasonable. This data suggests that the higher Indium content does not give significantly better noise figure than the existing material; however, reducing the gate length does give improved noise figure. The lack of noise figure improvement with the device with the highest In content (~20%) is surprising at first. We believe that that the limit for In content in a pHEMT has been surpassed by this device and channel electrical properties have degraded due to the formation of dislocations.

TABLE 2
Minimum noise figure, Fmin, and associated gain, Ga, measured on 4x50 μm devices at 8 GHz. The bias point is Vds=2.0 V and Id=50 mA/mm.

Case	Fmin (dB)		Ga (dB)	
Number	Average	Range	Average	Range
1	0.36	0.04	15.1	0.7
2	0.34	0.05	14.5	1.0
4	0.34	0.08	14	1.3
5	0.25	0.11	14.9	1.1
6	0.32	0.07	12.5	1.4

To evaluate the device power performance, experimental devices were assembled into jigs with tunable input and output matching networks. Table 3 shows a summary of the power performance data. For each case, several devices were tuned. Because of the large difference in breakdown voltage and maximum current between the different device types, devices were tested at different drain biases as appropriate. As shown in the table, similar output power and efficiency were obtained from the standard power device (Case 6) and the double recessed 0.25 μm low noise device (Case 4) at a drain bias of 7 V. The experimental material with "medium charge" (Case 2) also shows similar power, but lower efficiency. This may be due to the lower breakdown voltage of this device. The millimeter-wave material (Case 1) is inferior at X-band—power and efficiency both appear to be limited by the low breakdown voltage. The double recessed low noise devices with 0.15 μm (Case 5) have similar output power at 7 V, as we expect since the material is the same as

the 0.25 μm double recessed low noise device. However, efficiency is lower, and we were unable to tune devices at Vds = 9 V without burning them out. This may indicate a different breakdown mechanism associated with the shorter gate.

Based upon the measured data, the best candidates for use in both power amplifiers and low noise amplifiers are the standard 0.25 μm power devices (Case 6) and the double recessed 0.25 μm low noise devices (Case 4). They have very similar optimum-tuned power characteristics (27.7-27.9 dBm power, 60-63 % PAE, 11-11.3 dB gain at 8 GHz for an 8 μm x 100 μm device) for bias conditions of Vds = 7 V and Id = 50 mA/mm. Their minimum noise figures are also very similar as shown in Table 1. The double recessed low noise device has higher associated gain of 14 dB at 8 GHz.

TABLE 3.a
Tuned power performance measurement results for discrete 8x100 μm devices at the nominal drain voltage for the given material structure.

Case Number	Vds (V)	Pout (dBm)	Gain (dB)	PAE (%)
1	5	24.6	12.2	46.3
2	7	27.4	11.6	56.4
4	7	27.7	11.3	60.2
5	7	28.2	10	47
6	7	27.9	11	63.2

TABLE 3.b
Tuned power performance measurement results for discrete 8x100 μm devices at the highest possible drain bias.

Case Number	Vds (V)	Pout (dBm)	Gain (dB)	PAE (%)
1	6	25.6	11.9	48.7
2	9	28.8	12.4	52.8
4	9	29.0	11.7	56.8
5	8	28.1	10.7	41.5
6	9	29.3	11.4	56.5

MMIC RESULTS

X-band power amplifier MMIC and an X-band low noise MMIC amplifiers were processed using the standard 0.25 μm power process (Case 6). A chip layout for the power amplifier is shown in Figure 3. The power amplifier is a two-stage design with a 3.5:1 2nd stage to 1st stage FET ratio. The chip measures approximately 3.3 mm x 2.7 mm and delivers 4.5 W output power over a 2 GHz bandwidth at X-band frequencies. Since the standard power process was used in the design, it is not surprising that good power performance was achieved for the power amplifier.

X-band low-noise amplifier was also designed and fabricated using the same standard 0.25μm power process. The circuit consists of four identical stages of amplification. It used a single drain voltage for biasing. The chip measures approximately 4.0 mm x 2.2 mm and has greater than 32 dB of gain across more than 2 GHz of bandwidth. In addition to the good gain performance, the LNA also exhibits excellent noise performance at X-band frequencies. The measured noise figure, again covering more than 2 GHz of bandwidth, is well below 2 dB.

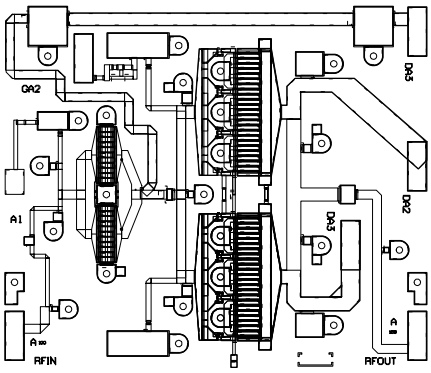


Figure 3. Layout view of X-band power amplifier.

CONCLUSIONS

Experimental data has been presented that advocate the use of a single double recessed pHEMT device for application as both high power amplifiers and low noise amplifiers. This finding has significant impact for cost reduction in manufacture of pHEMT devices at X-band. We believe that the same trend will hold at higher frequencies of operation for pHEMT devices.

ACKNOWLEDGEMENT

The authors would like to thank the technical staff and the management team of Raytheon RF Components for their expertise in wafer processing and continuous encouragement during the course of this work.

REFERENCES

1. M. Cardullo, C. Page, D. Teeter, and A. Platzker, IEEE MTT-S International Microwave Symposium Digest, 1994, vol.2, Pages: 801-804

2. P.K. Ikalainen, IEEE Microwave and Guided Wave Letters, vol. 6, 1996, Pages: 7-9