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Double distributed GaAs P-HEMT ICs for 40 Gbit/s high output voltage driver modules

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A 40 Gbit/s driver, based on two cascaded double-distributed amplifiers has been designed and realised for driving lithium niobate modulator. The ICs were fabricated with the 0.15 µm gate length GaAs P-HEMT technology from Philips OMMIC. The driver module exhibits a state-of-the-art output driving voltage of 8 Vpp, in 50 Ω load, and more than 26 dB gain over a 26 kHz to 43 GHz bandwidth.

Introduction: To get very high bit rate (several Tbit/s) in Dense Wavelength Division Multiplex (DWDM) optical transmission systems, 40 Gbit/s appears to be an appropriate bit rate per wavelength; this bit rate is to be obtained by Electrical Time Division Multiplexing (ETDM) because of very high speed electronic availability (SiGe, GaAs and InP). These three technologies have now demonstrated circuits operating at 40 Gbit/s and up to 80 Gbit/s for InP microelectronic [1]. In long haul optical transmission systems, electro-optic lithium niobate modulators are mainly used due to their very low chirp and high extinction ratio; but a high driving voltage (more than 6Vpp) is needed. Such characteristics imply a high breakdown-voltage*Ft product for the driver transistors and only GaAs or InP technologies can provide it; 40 Gbit/s commercial GaAs amplifier are actually available (SHF 806P) but not with such an output voltage over such a bandwidth.
This paper presents the design and realisation of driver circuits; it is based on an original double-distributed architecture circuit and is realised with the new high performance 0.15 µm GaAs P-HEMT technology developed by Philips OMMIC in France. Cascading two such circuits, a 40 Gbit/s module has been assembled and tested with a 40 Gbit/s Sumicem lithium niobate modulator. An output peak-to-peak voltage of 8 V was measured on 50 Ω which is, at our knowledge, the state-of-the-art in this domain [2], [3].

Circuit design: The driver consists in two chips: a divider-preamplifier (D-P) and a power-amplifier (P-A); to get a high output voltage in the power-amplifier, the basic idea is to put two distributed amplifiers in parallel to add their currents in a single common drain-line; for this purpose, the power amplifier includes two input gate-lines and a common high current drain-line while the divider-preamplifier has a single input gate-line and two output drain-lines to launch the signal into the two gate-lines of the power amplifier. Both circuits are using the well-known cascode-cells that allow a good input-output isolation. The power amplifier includes 2 times 10 cascode-cell stages while 2 times 5 cascode-cell stages are sufficient for the divider-preamplifier.
The driver module is realised by cascading the two circuits with two broadband by-pass capacitors (Fig.1) to solve the DC offset problem.

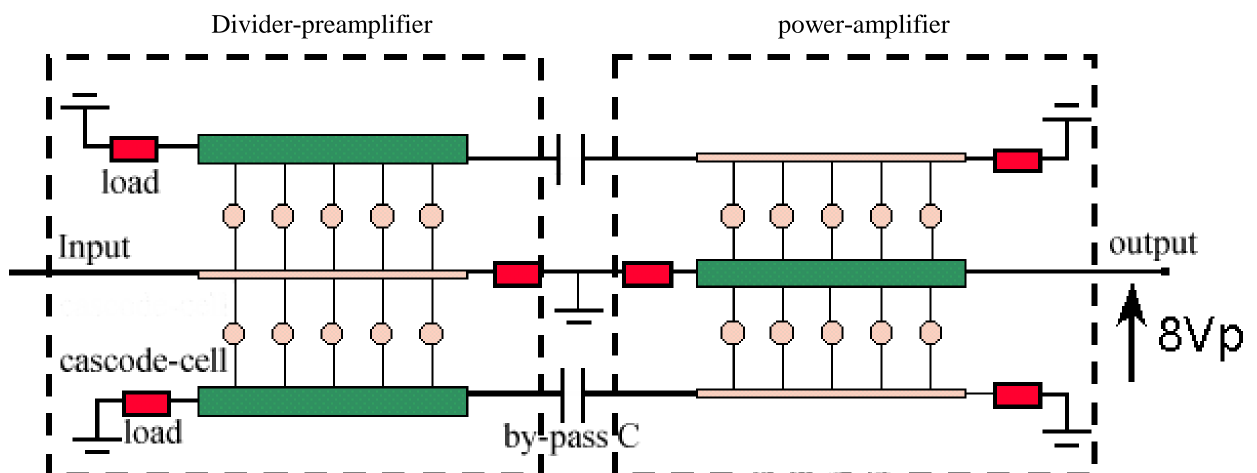

Fig. 1: Schematic circuit of the two-stages driver

The use of small transistors (about 30 µm width) allows, for a high gain, to keep good input and output matching. Due to high reliability of via hole technology, the microstrip line was preferred for its better ground plane definition. To get high stability over the whole bandwidth and keep a low consumption, a new high performance active 50 Ω load has been developed; one of the main advantages of this load is to guarantee a better gain stability against bias variations and temperature while allowing a fine output voltage adjustment. In the divider-preamplifier, as the drain current is smaller,

a classical resistor is used for lines terminations; this allows a dynamic gain adjustment of 6 dB without significant bandwidth reduction. Figure 2 shows the on-chip measurements of S21 parameters for both divider-preamplifier (a) and power-amplifier (b) respectively.

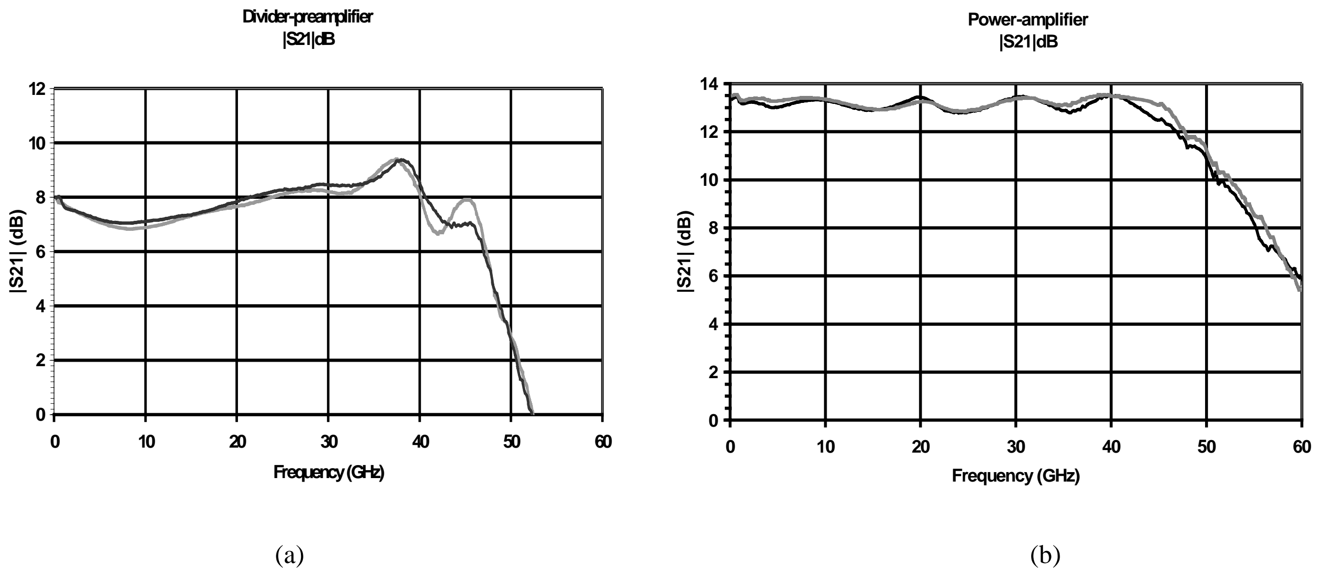

Fig. 2: On-chip measurement of S21 parameters of both divider-preamplifier (a) and power-amplifier (b)

For the divider-preamplifier (a), S21 parameters are measured between the common input gate-line and each of output drain-line while for the power-amplifier (b) S21 parameters are measured between each input gate-line and the common output drain-line. For the power-amplifier, results show a mean gain of 13.4 dB for each input-output gain then, as the two curved are practically superimposed, a total gain of 19.4 dB with an in-band ripple of 0.5 dB over a 3 dB bandwidth of 50 GHz is obtained; for the divider-preamplifier, a mean gain of 8 dB is measured over a 3 dB bandwidth of 48 GHz but the total inband ripple is about 2 dB; however, this can be equalized in the module.
Fabrication: Both ICs have been fabricated using the GaAs 0.15 µm pseudomorphic HEMT technology from Philips OMMIC. With a mushroom gate, the transistor has a threshold voltage of −0.7 V, a breakdown voltage of 11 V, a transconductance of 762 mS/mm, a transition frequency of 98 GHz, an Idss of 408 mA/mm at Vgs=0 and up to 730 mA/mm for Vgs=+0.7 V. This allows, for the power-amplifier, a maximum input swing voltage of 1.2 Vpp on each gate-line; this means that a theoretical output voltage of 11Vpp could be obtained. We have measured up to 8 Vpp with 0.4 Vpp at the input of the module which has a 26 dB gain. Figure 3 shows the circuit gain dispersion on a 3" wafer.

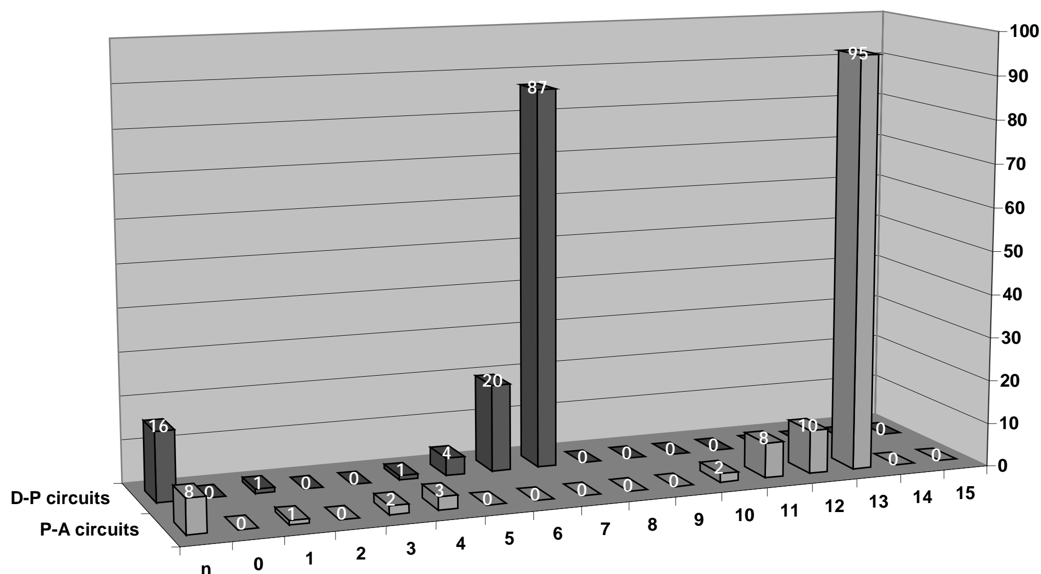

Fig. 3: Circuit gain dispersion on a 3" wafer

For a total of 129 measured circuits each, 113 power-amplifiers are in the designed specifications (87.6%) and 107 (83%) for the divider-preamplifier. The dispersion is very tight centered around 13.4 dB for the power-amplifiers and 7.5 dB for the divider-preamplifiers.
The cascaded circuits have been reported on an alumina substrate and incorporated in a very small cavity package to realise a driver module with the above mentioned characteristics. The total power consumption is 2.5W for 12V DC bias.
A pseudo-random 40 Gbit/s NRZ pulse stream output from a SiGe based MUX from Alcatel-Stuttgart was applied to the module input; the output was adjusted to 6 Vpp to match with the HF Vpi of a Sumicem lithium niobate modulator; clear electrical and optical eye-diagrams were obtained (Fig 4).

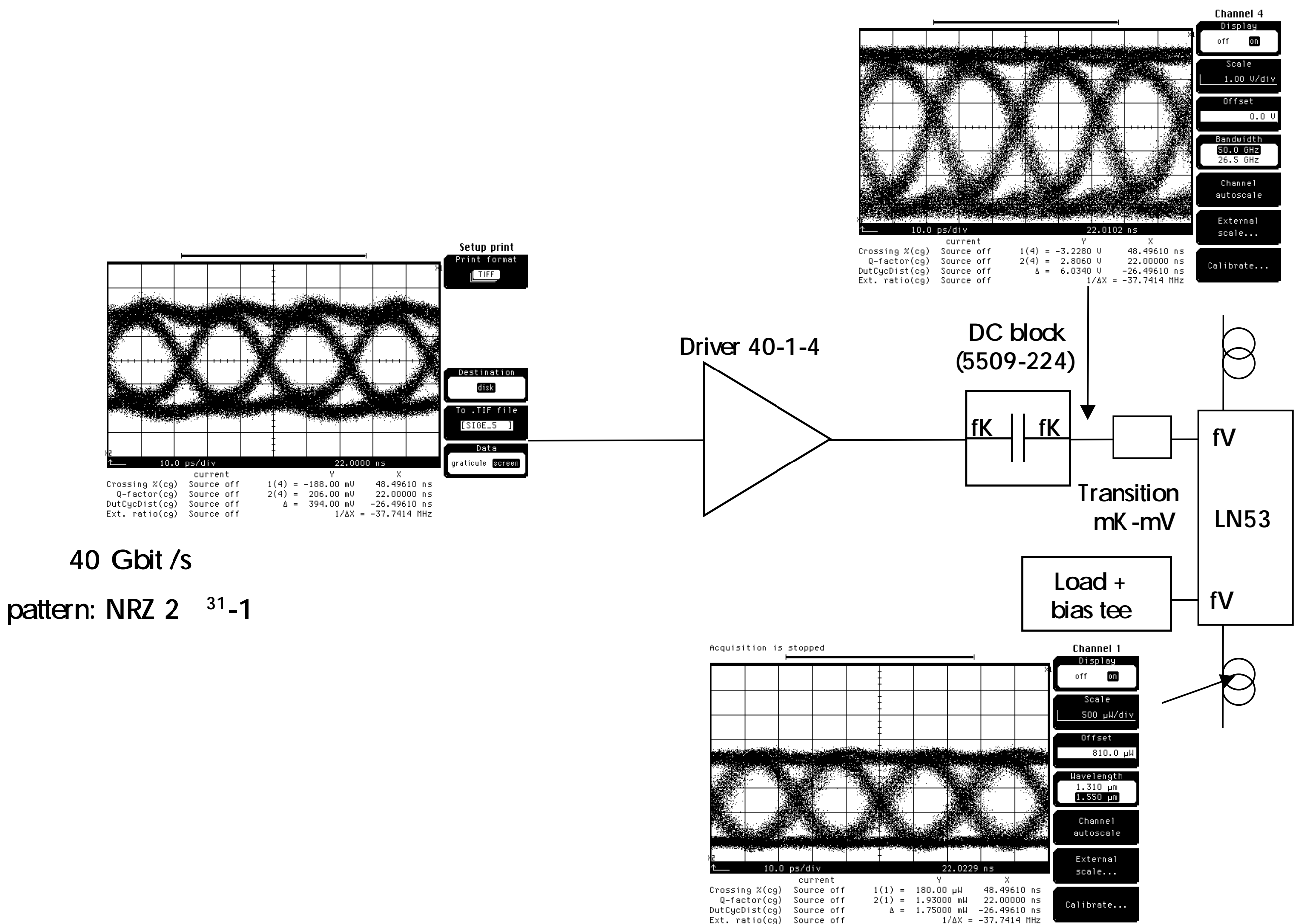

Fig. 4 : Measurements on driver module showing electrical eye-diagrams at 40 Gbit/s at the input and output of the driver and the obtained optical eye-diagram obtained at the modulator output.

Conclusion: High speed driver circuits, based on an original double-distributed architecture, have been designed in OPTO+ and realised with the 0.15 µm GaAs P-HEMT technology from Philips OMMIC. The maximum total gain obtained on the module is 26 dB which is very close to the total gain measured on the wafer for the two circuits (27.5 dB). The measured bandwidth ranges from 26 kHz up to 43 GHz and the output voltage obtained on 50 Ω is 8 Vpp. These are state-of-the-art results for such circuits and driver modules. For long haul optical transmission system applications, these technology and circuit architecture are very promising approaches.

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