# Manufacturable Commercial 4-inch InP HBT Device Technology

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**Abstract**

**A manufacturable, reliable, and high performance InP Heterostructure Bipolar Transistors device technology (SHBT and DHBT) has been developed and being offered for commercial foundry services. These devices are ideal to provide a complete chipset for 40 Gb/s fiber optic communication (OC-768) as well as high performance power amplifiers for 3G wireless applications. A peak cutoff frequency, $F_t$, of over 200 GHz was obtained for non-self aligned 1X3 $\mu m^2$ device. The devices were designed for high reliability by employing an Al-free (InP) emitter and a carbon-doped base. Excellent device yield and uniformity observed across the wafer clearly demonstrated the feasibility of this technology for MSI-level of integration required in MUX/DMUX communication circuits.**

## INTRODUCTION

The advent of OC-768/STM-256, or 40 Gbps, optical communication systems has set forth stringent performance requirements on the device technology for the electronic components and sub-systems: high frequency, low power, and medium-scale integration. Intrinsic material advantages, such as high electron mobility and low turn on voltage, have made InP-based HBT the natural choice for high-speed and low-power digital circuits [1-5]. Over the years, circuit designers have exploited the advantages of InP HBT to design ultra-high performance circuits for various military applications [1], [6]. However, due to the low volume required of these applications, issues critical to the manufacturability of InP HBT have not been pursued rigorously. Recently, GCS has successfully demonstrated a high-performance InP HBT technology for commercial pure-play foundry services.

With a proprietary device design and fabrication process technology, we have addressed the challenge of manufacturability and reliability of InP HBT technology in a fundamental way. The InP HBT baseline process is designed to be synergistic with our current production-ready InGaP/GaAs HBT process. GCS's InP HBT technology uses a novel epi design with an InP emitter and a carbon-doped base to ensure long-term reliability. A high-yield, low-loss interconnect technology has also been developed for high-speed InP HBT circuits. Another feature of this proprietary process is that the emitter width is scalable to sub micron size. This scalability enables further optimize of the device performance in the future by reducing device geometry and power dissipation while increasing the circuit speed. By offering both DHBT and SHBT devices, GCS enabled the designers to design a complete 40Gbps chipset that meet the requirements for low-power, high-speed (PMD) and high voltage drive (modulator drivers) chips.

## BASELINE FABRICATION PROCESS

Recent availability of high-quality 4-inches InP epitaxial materials from pure-play epi-vendors has enabled rapid development of InP HBT device technology for commercial applications. Leveraging from our production-ready InGaP/GaAs 4-inch HBT line, we have developed an InP HBT baseline process that take complete advantages of the maturity of the various process modules developed for GaAs-based HBT (photolithography, thin film, etch modules, etc).

The current baseline process employed industry-standard production stepper (Canon I-line stepper) to define all photolithography steps. Key features of GCS's InP HBT process are: mesa-etched isolation and planarized process using a low permittivity dielectric; low-loss multiple levels interconnect; and high yield, non-self aligned devices with minimum emitter width of 1μm. Systematic and aggressive development has enabled us to attain very tight control in critical dimensions (CD) and patterns alignment, hence devices and circuits yield. Low damage wet etchings with designed-in selectivity etch-stops were utilized to maximize device uniformity and reproducibility. A proprietary passivation technique has been developed and demonstrates to dramatically improve the device reliability. Furthermore, to enhance the manufacturability of InP HBT technology, we have designed our baseline process to be applicable to both SHBT and DHBT. Only at a few critical etch steps, the DHBT wafers were routed to be processed differently.

The passive components in the InP HBT technology are identical to those in our InGaP/GaAs HBT process (i.e. thin film resistors, MIM capacitors, etc). However, in order to minimize undesirable resistance and maximize circuit yield, we have developed a planar, low-loss interconnect for InP HBT. Often overlooked in device technology development, interconnects plays a critical role in the yield and

manufacturability of MSI and LSI circuits. With our proprietary fabrication process, reproducible and high yielding interconnects have been routinely fabricated.

## DEVICE PERFORMANCE AND MODELS

### *DC Characteristics*

Engineering trade-offs between device performance and yield have been systematically investigated to synthesize our baseline epitaxial material structures and fabrication process. A summary of GCS's baseline device specifications is shown in table I. Our current SHBT process, which is tailored for low power and high frequency circuits, offered 3 standard device cells (1X3, 1X5, and 1X10 $\mu m^2$ emitters). A nominal common-emitter current-voltage of a 1X3 $\mu m^2$ is shown in Figure 1.

TABLE I
GCS InP HBT BASELINE DEVICE SPECIFICATIONS

| Device Parameter | InP SHBT | InP DHBT |
|---|---|---|
| Beta | >30 | >30 |
| $BV_{ceo}$ | >3.5V | >8V |
| $Vce_{offset}$ | <0.3V | <0.3V |
| $F_t$ * | >160GHz | >150GHz |
| $F_{max}$* | >160GHz | >150GHz |

* $F_t$, $F_{max}$ @ $J_c$=100kA/cm$^2$

As shown in Figure 1, the device characteristic is ideal for low-voltage applications, with an offset voltage of less than 150mV and a knee voltage of 500mV, thereby allowing the device to be biased into the active regime with $V_{ce}$ as low as 600mV. The device has a base-emitter and base-collector breakdown voltage of over 2V and 6V, respectively. A corresponding forward Gummel plot is shown in Figure 2. As expected, the leakage currents remain minimal down to very low $V_{be}$, indicating that the leakage contribution due to surface recombination is minimal.

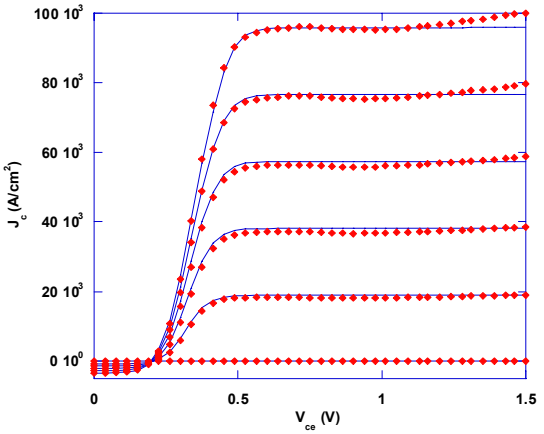


**Figure 1: Room temperature common-emitter characteristics of a baseline InP SHBT with 1X3 $\mu m^2$ emitter (Points are from the measurements and solid lines are from the model).**

A large signal Gummel-Poon models have also been developed for these devices. Shown in the plots (Figure 1 and 2) is the DC matching of the modeled and measured data for the device. Excellent agreements of both the common-emitter and forward Gummel characteristics over the entire bias range indicate that the model is more than adequate for high performance circuit designs and simulation. Discrete temperatures Gummel-Poon have also been developed to enable more accurate simulation of the devices in actual operations.

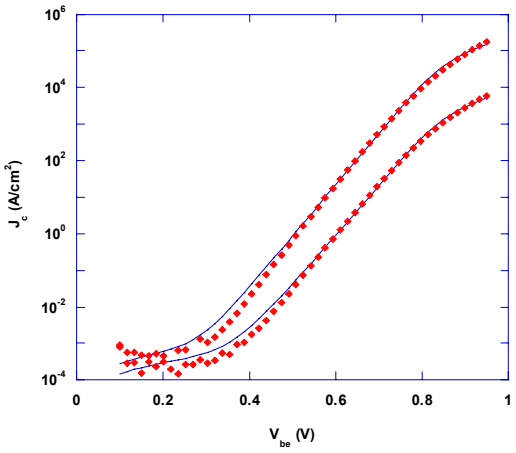


**Figure 2: Forward Gummel characteristics of a baseline InP SHBT with 1X3 $\mu m^2$ emitter (Points are from actual measurements and solid lines are from the model)**

### *RF Characteristics*

On-wafer S-parameter characterization of the devices were performed using an HP-8510. Shown in Figure 3 is the plot of $H_{21}$ versus frequency at a $V_{ce}$ = 1.0V and $J_c$ = 100 kA/cm$^2$. Extrapolation from 40Ghz, an $F_t$ of over 170GHz is obtained. The corresponding $F_{max}$ of the device at this bias condition is ~160GHz.

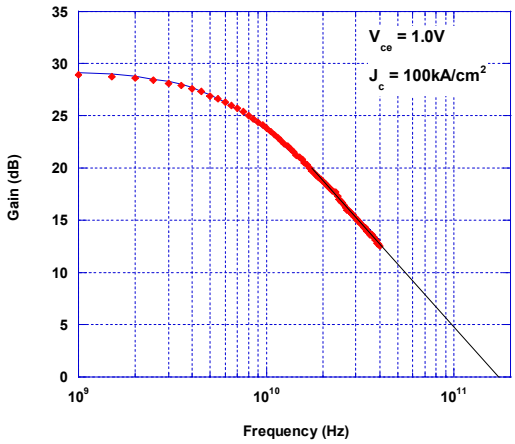


**Figure 3: $H_{21}$ versus frequency for an InP SHBT with 1X3 $\mu m^2$ emitter. Extrapolation yields a cut-off frequency of ~170GHz. (Points are from actual measurements and solid lines are from the model)**

Biasing the device at higher current densities, $J_c$=160kA/cm$^2$, an $F_t$ >200GHz is extrapolated (Figure 4). These RF figures of merits, along with the low bias conditions clearly demonstrated the suitability of InP SHBT for low-power, high speed digital circuits, at 40Gbps and beyond.

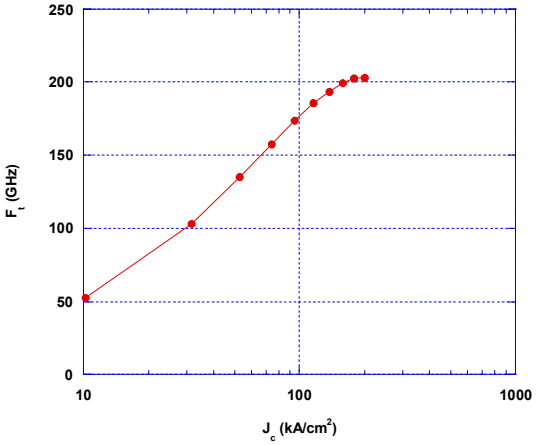


**Figure 4: Ft versus Jc characteristics of an InP SHBT with 1X3 μm$^2$ emitter. An Ft of ~200GHz is obtained at Jc=160kA/cm2.**

## RELIABLE PROCESS DEVELOPMENT

Due to the relative immaturity of InP HBT device technology, critical issues related to the concerns of reliability have not been addressed rigorously. Yet, reliability is of paramount importance in systems, circuits, and devices for commercial digital communication applications (where the systems are on most of the time). Over the years, scattered publications on reliability study of InP HBT have been published [7-9]. Conclusive data on the issues of reliability of InP HBT device technology remained unresolved. We are addressing the reliability issues of InP HBT in a fundamental way, through fast fabrication cycle-time and rapid feedback measurements. These short-loops enable us to quickly resolve the reliability issues related to the processing or epistructure of the devices.

Using integrated process design, our InP HBT baseline devices have been developed with reliability concern in mind from the very beginning. Starting from the epitaxial structures to the fabrication processes, awareness of potential reliability issues has been paid close attention to. An Al-free InP emitter (instead of AlInAs emitters) and carbon-doped base (instead of the commonly used Be) have been employed in the device epistructure to improve reliability. A non-alloyed Ohmic metal contact scheme has been developed to enhance the robustness of the devices under high current drive.

A proprietary passivation technology has been developed to ensure surface cleanliness and enhanced reliability for our InP HBT technology. As shown in Figure 5, dramatic improvement in term of the device stability is observed in device that has been passivated with this process compared to a device that has not been optimally passivated after 1 hour of stressing at high current density ($J_c$=150kA/cm$^2$) and elevated temperate ($T_j$ = 294°C). With this passivation, very reliable InP HBT could be fabricated.

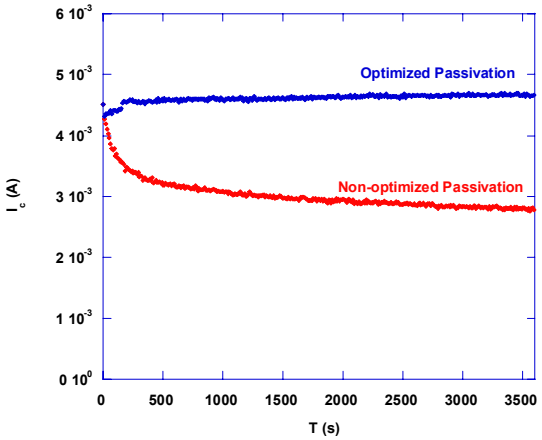


**Figure 5: Stress test of InP HBT devices with and without passivation for InP SHBT.**

High temperature over life (HTOL) reliability testing at nominal operating condition ($V_{ce}$=1.0V and $J_c$=100kA/cm$^2$) has been performed on our InP SHBT. Preliminary data of the on-going test is shown in Figure 6. The devices are shown to be very stable at the current >100 hours stressing. The initial drop in current gain shown in the plot is being investigated. We believe that it can be eliminate.

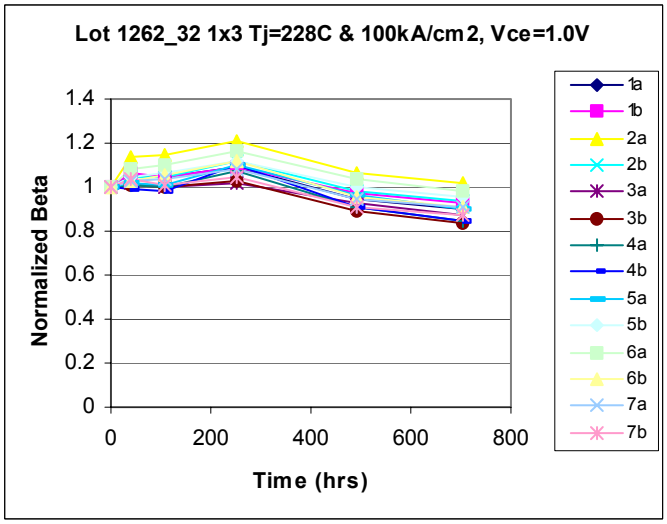


**Figure 6: HTOL testing of a 1X3 μm$^2$ InP SHBT at $T_j$=228°C ($V_{ce}$ = 1.0V, $J_c$= 100kA/cm$^2$) after 1 hour burn-in. Stable gain is observed after 700 hours of stressing.**

## CONCLUSIONS

We have developed a manufacturable, reliable, and high performance InP HBT device technology (SHBT and DHBT) for commercial foundry services. The InP SHBT exhibits excellent frequency performance with a peak $F_t$ >200 GHz at 160kA/cm$^2$. Proprietary device and process design has produced robust and reliable devices. Preliminary HTOL testing yielded stable device characteristics after >100 hours of stressing. These devices are ideal to provide a complete chipset for 40 Gb/s fiber optic communication (OC-768) as well as high performance power amplifiers for 3G wireless applications.

## ACKNOWLEDGEMENTS

The authors would like to thank Kevin Feng and Mike Brunsman for their helps with device characterization, modeling and reliability testing. Additionally, support from the manufacturing operation is much appreciated.

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## ACRONYMS

InP: Indium Phosphide
SHBT: Single Heterostructure Bipolar Transistor
DHBT: Double Heterostructure Bipolar Transistor
HTOL: High Temperature Over Life