A Non-Self Aligned InP HBT Production Process

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Abstract

An InP DHBT process technology implementing commercial carbon-doped epitaxial structures has been developed and characterized in a high volume 4-inch wafer production line. This HBT technology utilizes non-self aligned emitter and base contacts, InP emitter, selective etch stop layers and optimized base-collector junction grading profile for enhanced manufacturability and performance. The availability of high quality and stable InP-based commercial epitaxial materials has greatly shortened the process development time. Our InP DHBTs exhibit very low knee voltage of 0.5V at 100 kA/cm^2 with peak ft= 160 GHz and peak fmax of 190GHz. A SPICE-like large signal model is also discussed in this paper. Following the successful pattern of its GaAs HBT counterpart, we believe a low cost, high yield and manufacturable 4-inch InP HBT production will become a reality soon.

Introduction

Due to the recent economic slowdown and capital spending reduction, communication industries including system houses and component companies are all suffered with significant revenue loss and reduce R&D spending. However, at Alpha Industries we believe the thirst for the higher data rate has not been quenched. The needs for the better and less expensive communication systems will still thrust for many years to come. Therefore Alpha continues to invest the technologies to enable the performance enhancement and cost reduction for the current and next generation wireless and broadband communication markets. By leveraging our existing high yield and high performance InGaP HBT production experience, an InP HBT technology is developed in a very short period of time and soon to be released to engineering production.

InP DHBTs offers numerous advantages over other competing technologies for the applications of high-speed communication. In our view, the most attractive features are the lower power consumption due to their low turn-on voltages, higher Johnson's limit due to high breakdown of InP collector, moderate circuit integration level up to a few thousand transistors and the potential to integrate with optoelectroic devices such as photodetectors. These features have rendered the InP DHBT technology as a strong candidate for fabricating a complete low power transceiver front-end chipset such as laser diodes drivers (LDDs), transimpedance amplifiers (TIAs), limiting amplifiers (LAs), multiplexers (MUXs), demultiplexers (DeMUXs) and clock data recovery (CDRs) circuits for next generation communication systems.

InP DHBT Epitaxial Structure

To address the device performance as well as the manufacturability, an InP/InGaAs/InP DHBT epitaxial profile was designed to take advantages of the ballistic transport of InP emitter launcher and the wet etch selectivity between the emitter and base layers. Each wet etch step in our process has an etch stop layer to ensure excellent etch uniformity across a 4-inch InP wafer. A proper treatment of base collector junction has been employed to minimize the current blocking effect. A schematic cross sectional profile of such a generic InP DHBT is shown in figure 1.

N+ GaInAs Contact
N+ InP Emitter Contact
n InP Emitter
UD GaInAs spacer
P+ GaInAs Base
Grading Layer
n InP Collector
N+ GaInAs Etch Stop
N+ InP Subcollector
N+ GaInAs Etch Stop

Figure 1: A schematic cross-section of a generic InP DHBT layer structure.

This InP DHBT structure can be easily tailored to meet different frequency bandwidth requirements by varying the InGaAs base and InP collector thickness.

InP HBT Device Process Technology

To achieve optimal performance, most conventional InP HBT technologies utilize a so-called self-aligned process to reduce unwanted parasitics, such as base resistance R_b and base-collector capacitance C_{bc}. However, the self-aligned approach often compromises circuit yields and integration levels, which are important factors in manufacturing environments. As the active device areas scaling down to reduce power consumptions, it becomes even more challenging to achieve a high yield self-aligned process. At Alpha Industries we have developed a non-self aligned InP DHBT technology with great success. With a highly accurate alignment lithography capability, this non-self-aligned process can achieve consistent critical dimension control between the emitter and base contacts, and therefore the devices can have low parasitics and enhanced rf performances. The process implemented includes the formation of the three critical contacts (emitter, base, and collector) with the proper ohmic contact metallization, mesa-etch device-to-device isolation, NiCr thin film resistor, MIM capacitor, multi level metal interconnects, and the final nitride encapsulation. Figure 2 (a) shows a SEM X-section of a fabricated InP HBT device with a 0.3 µm of ledge. Figure 2 (b) is a blow-up photo of the emitter and base contact area.

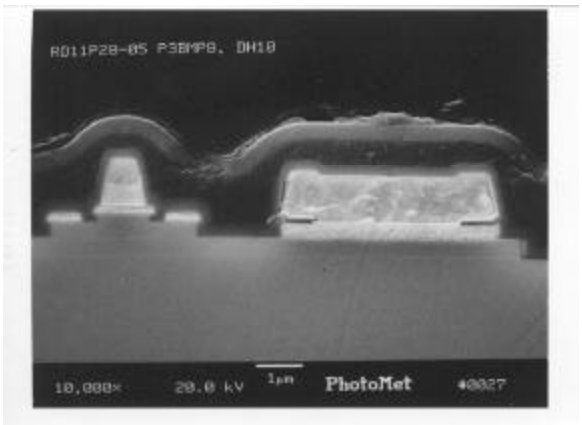

Figure 2 (a): SEM cross-section of a non-self aligned 1.2x8 μm^2 InP DHBT

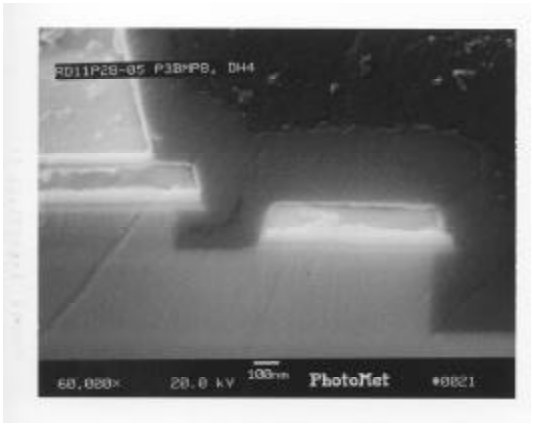

Figure 2 (b): A blowup of emitter and base contact area of the InP HBT device shown in figure 2 (a).

This InP HBT front-side process is very similar to Alpha's high performance InGaP HBT process which has been demonstrated for various circuit fabrications with high yield and high integration capability. As a matter of fact, this InGaP HBT digital process has successfully yielded various transceiver front-end circuits such as LDDs, TIAs, LAs, MUXs, DeMUXs integrated with CDRs for OC-192 (10Gb/s) fiber optic applications [1]. High yield and high integration capability are demonstrated on the success of fabricating a direct digital synthesizer (DDS) circuit designed by Rockwell Colin as shown in figure 3 with a chip size of 4 mm by 4mm and an greater than 8000-transistor integration level [1].

Our InP HBT and InGaP HBT technologies share the identical back-end process, such as passive NiCr resistors, MIM capacitors, spiral inductors and metal interconnections, which are in general the primary yield limiting factors in a GaAs-based HBT technology. Therefore, we expect this InP HBT technology to show similar circuit yields and integration levels as our InGaP HBT technology. For manufacturing it is critical to implement SPC charts to ensure the equipment control at optimum conditions. A set of process monitors are also generated and monitored during the processing. These monitors are not only used to control the process but also are used to monitor the key device parameters. Typical passive parameters for HBT fabrication include the ohmic contact resistances for emitter, base and collector, the implanted isolation sheet resistance, metal line resistances, metal to metal contact via resistances, NiCr resistance and MIM capacitance. Due to the vertical topology nature of HBT and associated negative etching profile, the monitor of inter-level metal line continuity and its step coverage is also included.

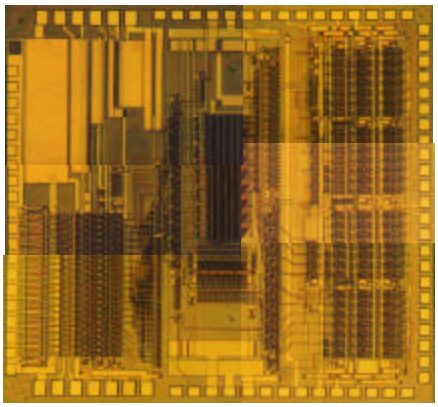

Figure 3. A photograph of a fabricated Direct Digital Synthesizers using Alpha's InGaP HBT technology with ~ 8000 transistors and a 4 mmx4 mm chip size.

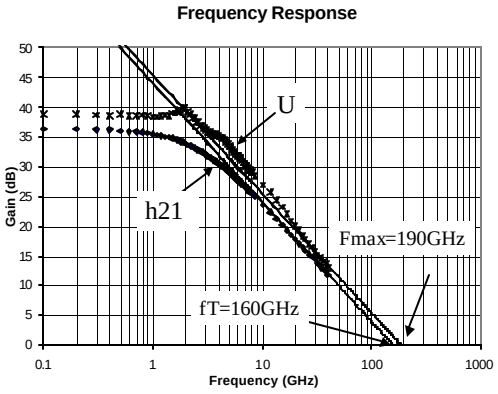

Figure 5: Frequency reponse of 1.2x8μm^2 InP DHBT at Ic=18 mA and Vce = 2V

DC and RF Characteristics

As can be seen in figure 4, the common emitter I-V characteristics of a typical 1.2x8 μm^2 InP DHBT shows little sign of current blocking effect. At a current density Jc of 100kA/cm^2, the knee voltage is only around 0.5 V. This indicates that the properly designed grading layers between the base and collector junction have effectively eliminated the conduction band spike. This generic InP DHBT structure can be easily tailored to meet different frequency bandwidth requirements. For OC-768 fiber optics communication applications, with a 200 nm n- InP collector, the rf performance for a typical 1.2x8 μm^2 discrete device characteristics is shown in figure 5 and 6 with peak ft= 160 GHz, fmax of 190GHz and breakdown voltage BV_{ceo} ~7V. Even at Jc=50KA/cm^2, f_T over 100GHz and f_{max} over 130GHz are obtained.

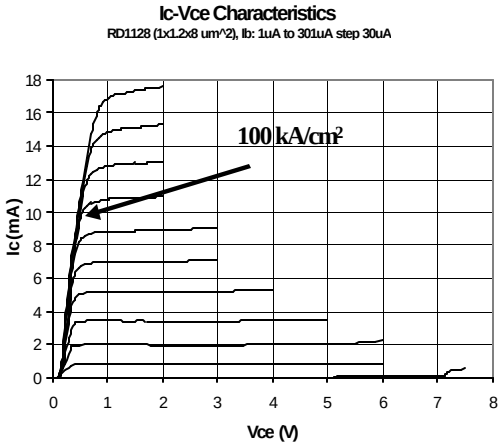

Figure 4: A typical common-emitter I-V of 1.2x8μm^2 InP DHBT

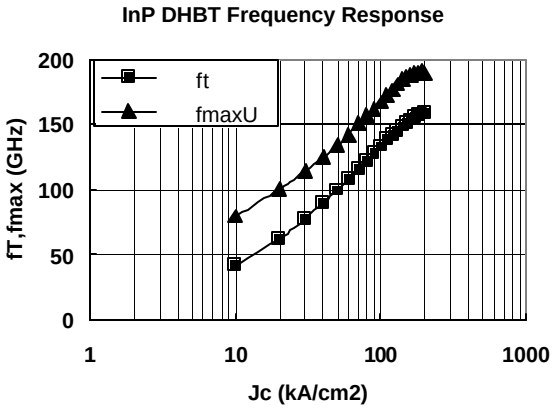

Figure 6: f_T and f_{max} vs. collector current density at V_{CE} =2V

Device Modeling

A SPICE-like large signal model modified from the standard GP model has been developed for the InP DHBT. This model can be implemented in popular commercial circuit simulators such as Pspice and ADS. Since the developed InP DHBT technology significantly reduced the current blocking effect in the base-collector junction, a similar circuit topology as used in our InGaP HBTs [1] can be employed in the device modeling without sacrificing accuracy. Figures 7 and 8 show the comparison of modeled and measured I-V characteristics with constant Vbe driving and constant Ib driving, respectively. As shown in the figures, good agreements between modeling and measurement have been achieved. Although the thermal conductivity of InP substrate is better than that of GaAs substrate, we found the self-heating is still an important issue in the device modeling. The junction temperature rise

induced by self-heating leads to the reduction of the emitter junction built-in potential and the increase of the reverse hole injection from base to emitter [2]. As can be seen in figure 7, the collector current of the InP DHBT tends to run away as the DC power rises. This is similar to those observed in GaAs-based HBTs, indicating the reduction of the emitter junction built-in potential with the rise of junction temperature. On the other hand, as shown in figure 7, the Ib driven I-V family curves do not show negative resistance as usually seen in GaAs HBTs, implying the reverse hole injection from base to emitter is less dependent on the junction temperature in InP HBTs. Our HBT model simulates the extent of the two effects separately and achieves accurate modeling results for both I-V characteristics. Besides the thermal issue, if the current blocking in the base-collector junction is significant, the barrier effect in the BC junction of a DHBT should be modeled properly in order to achieve a good accuracy across the full bias range of operation.

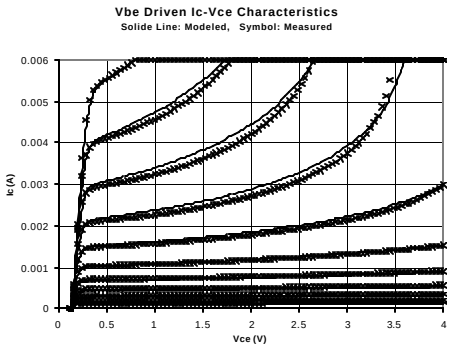

Figure 7: Vbe driven I-V characteristics of 1.2x8μm^2 InP DHBT InP DHBT

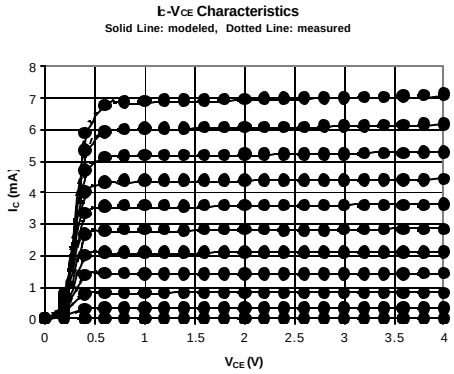

Figure 8: Ib driven I-V Characteristics of 1.2x8μm^2 InP DHBT

Conclusions

We have developed a manufacturable and high yield InP DHBT process technology by leveraging our InGaP HBT production experience. The technology has produced InP DHBTs, which demonstrated a peak ft of 160 GHz and fmax of 190 GHz with breakdown voltage BV_{ceo} ~7V. InP DHBT technology is a strong candidate to fabricate low power high-speed transceiver front-end chip sets, which are essential for the next generation communication systems. The successful development of the InP HBT technology will place Alpha Industries in a good position to capture the future high-speed chipset market by offing fast turnaround, low cost, and high performance circuits as soon as the market is ready.

Acknowledgements

The authors would like to express the appreciation to Euvis Inc., and Rockwell Colin for technical discussion and contributing data and information for this paper.

References

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ACRONYMS

DHBT: Double Hetero-junction Bipolar Transistor
LDDs: Laser Diodes Drivers
TIAs: Transimpedance Amplifiers
LAs: Limiting Amplifiers
MUXs: Multiplexers
DeMUXs: Demultiplexers
CDRs: Clock Data Recovery
DDS: Direct Digital Dynthesizer