

Accelerated Reliability Testing of InGaP/GaAs HBTs

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Abstract

Although InGaP/GaAs HBTs are usually reliable devices, their reliability can be compromised by processing or epitaxial material issues. Here we describe a number of techniques for determining the reliability of HBTs at accelerated rates compared with the normal three-temperature method. Some of these techniques show great promise for the rapid assessment of lifetime, which is especially useful for routine qualification of devices and for the rapid assessment of the suitability of processing or epitaxial material changes. Examples are chosen from epitaxial materials with both good and bad reliability.

INTRODUCTION

Reliability requirements for telecommunications applications are extremely stringent, typically <10 FITs in 20 years operating life. To ensure these requirements are met Nortel Networks HBT devices are tested:

- after any change in process that is likely to impact the reliability
- after any change in epitaxial material (vendor, reactor, precursors etc.)
- periodically to ensure reliability is unaffected by unforeseen changes.

Our standard method of reliability testing is to perform a three temperature (3T) accelerated test and predict the failure time at maximum junction temperature using an Arrhenius expression. These tests are usually performed at the maximum rated collector current density of 4.10^4 A.cm^{-2} . Unfortunately the maximum temperature of these measurements must be limited to avoid failure modes with high activation energies, which would not impact devices under normal operation [1,2]. Tests on good quality material can typically take more than a year, which is impractical in many instances. To circumvent this we have developed several new methods of reliability testing that can serve as quick indicators of potential reliability problems, although 3T tests are still our absolute standard.

THREE TEMPERATURE TESTS (3T TESTS)

We have found that reliable results can only be achieved if strict ESD precautions are observed, and the devices are not allowed to oscillate. Our 3T tests are performed using a

reliability coupon containing eight stabilized $2 \times 2 \mu\text{m}$ square emitter HBTs. These are eutectic bonded into packages and inserted into ovens held at 210, 243 and 268°C. Class I ESD precautions are observed throughout assembly and test. During stress individual transistors are biased at emitter currents of 1.6mA ($J_e=4.10^4 \text{ A.cm}^{-2}$), with $V_{bc}=0$. Gummel measurements are periodically performed at room temperature, and the Time To Failure (TTF) determined by a change in current gain (beta) of 20%. Using a lognormal

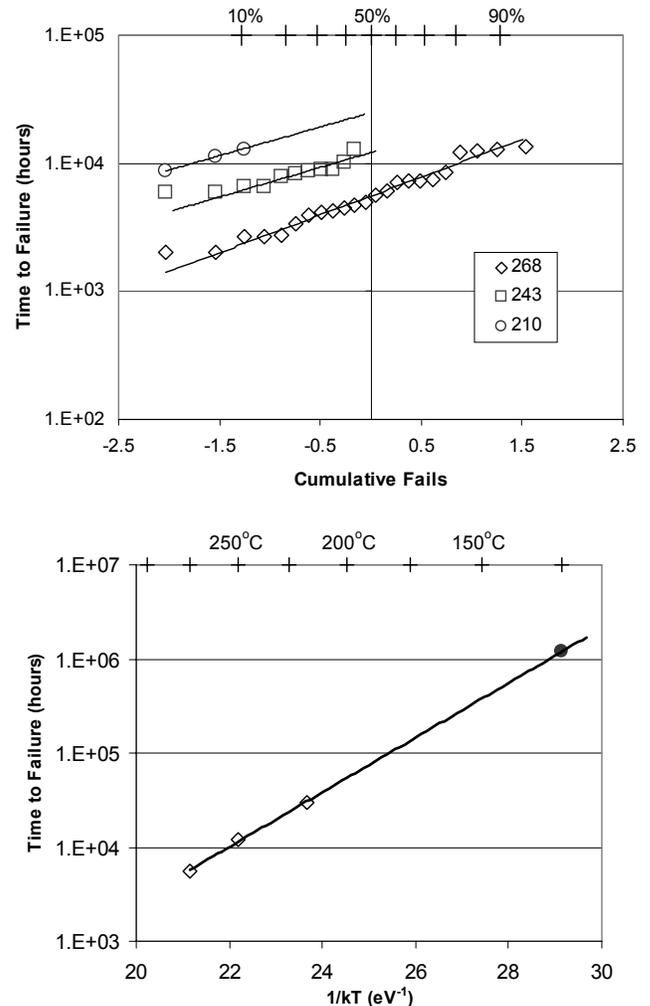


Figure1. CFD and Arrhenius Results From 3 temperature testing

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distribution we determine the Median Time To Failure (MTTF) and the sigma of each distribution from the Cumulative Failure Distribution (CFD), and determine the MTTF at 125°C and the activation energy (Ea) using the Arrhenius expression. A typical example of the results obtained from good devices is shown in figure 1. This methodology conforms to the JEDEC guidelines[3]. Lifetimes determined in this manner are typically around MTTF=1.10⁶ hours with a sigma<0.5 and Ea approximately 0.8-1.0eV, which gives a 20 year FIT rate of less than 10. However in this case the test has to continue for over 3 years in order to achieve even 50% fails at the lowest oven temperature. It is very unwise to predict MTTF unless at least 50% failures have occurred at all temperatures, as there always exists the possibility of a lower activation energy failure mechanism that could limit the lifetime of a device, and which may not show up until late in a study. Misleading MTTF predictions can also result if insufficient failures are achieved, especially if there are any defective devices.

Obviously test times of several years are not suitable for qualifying a new epitaxial wafer vendor, for example, and so methodologies have been developed to produce more rapid results.

HIGH CURRENT STRESS (J STRESS)

Very early in the development of our original AlGaAs/GaAs HBT process [4] 3T testing revealed the presence of a low activation energy failure mechanism on one wafer. To use 3T as a means of screening for similar wafers would have required many weeks of testing, which was obviously an untenable solution. It was discovered, by current step stress studies, that accelerated aging at very high current densities (around 5.10⁵ A.cm⁻²) with Vbc=0, could produce failures in this wafer in a few hours, whereas normal material would survive unaffected for many tens of hours, so a simple probed test of reliability coupons for 4 hours per device at this current (20mA for a 2x2um emitter device) was implemented on every production wafer. This test time allows 6 sites (48 devices total) to be tested per wafer in a 24 hour period. This test is also useful for revealing the presence of defective devices displaying early failures (or infant mortalities). Wafers are only used if no devices fail during the test period. Under these test conditions the junction temperature can increase by up to 80°C through self heating, which is not sufficient to degrade the life of normal devices to the extent observed, so obviously some degree of accelerated aging is caused by the increased current density. The generally accepted expression for lifetime is a power law in current:

$$MTTF = A \exp(Ea/kT) Je^{-n} \quad (1)$$

which is also the form of Black's Law for electro-migration. Here Je is the emitter current density, and Ea is the activation energy, and A is a constant for a given wafer.

Sugahara et al determined a value of n=2 for AlGaAs emitter devices [5]. Recently Feng et al have determined a value of 1.7 for AlGaAs emitters and of n=0.51 for InGaP emitters [6]. For our InGaP material a value of n~1 was determined from 7 wafers measured at 4.10⁴ and 8.10⁴ A.cm⁻². However, none of the studies mentioned above went to the extremes of current density used in our J-stress test.

When increasing the current appreciably above the operating current we have to beware of activating failure mechanisms not of concern under normal operation. Firstly we must ensure that the device does not start to display the Kirk effect. Secondly, we must ensure that the voltage drop across the collector resistance does not become large enough that the B-C junction becomes forward biased and the base current starts to increase significantly. To some extent both these concerns can be addressed by examination of the Gummel plots, which show no discernable discontinuity in base current for collector currents up to 20mA.

Further confirmation that collector voltage drop is not an issue can be obtained by comparing the CFDs of devices stressed with additional collector voltage applied, as shown in Figure 1. For a 2x2 transistor we estimate, by several other techniques, that the thermal impedance is ~2°C/mW, so at 20mA, the curves for 25°C, Vbc=1 and 65°C, Vbc=0, and the curves for 25°C, Vbc=2 and 105°C, Vbc=0 should be similar. The agreement between these plots not only confirms that the B-C junction is not overly forward biased, but also that increased collector voltage does not introduce any additional failure mechanisms other than increased self-heating.

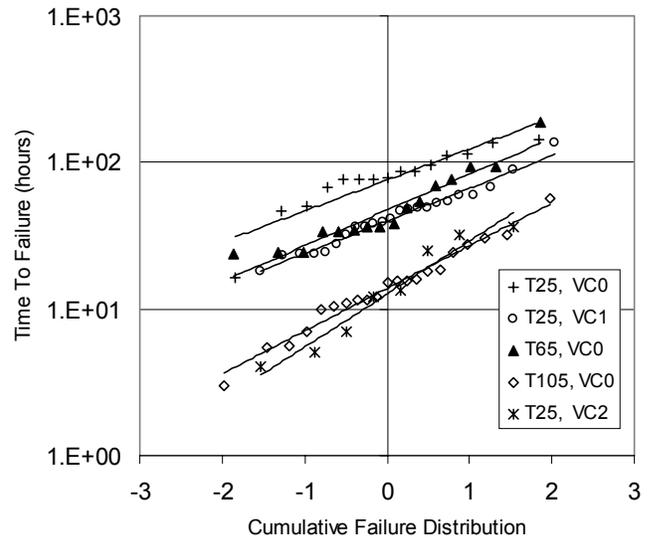


Figure 2. Comparison of Failure Times

Since implementing our InGaP/GaAs HBT[7], we have increased the collector voltage during J-stress to Vbc=1, to

increase the temperature of the devices and increase the likelihood of discovering wafers with poor reliability. This, to some extent, compensates for the reduced current acceleration obtained with InGaP emitters compared to AlGaAs.

CURRENT AND VOLTAGE STRESS (J-V STRESS)

Given the ability to accelerate failure by applying high currents, and increased voltage (a combination of current and temperature acceleration) it is tempting to see if a systematic variation could produce a reliability predictor for normal operation. One limitation to simply increasing the voltage to attain very high temperatures (apart from avoiding temperatures approaching alloy temperatures) is that the device breakdown voltage at high currents is significantly less than BV_{cbo} . We have examined the common base characteristics of our logic, standard, medium power and high power devices (with BV_{cbo} values of 10, 16, 22 and 30 volts respectively), and shown that in no case does this drop below 4-5 volts, even at emitter currents of 20mA. We can therefore feel confident that at the value of $V_{bc}=2V$ there is no possibility of breakdown occurring. Over the allowed current range of 0-20mA, and V_{ce} from 1.4 to 4 ($V_{bc}=0-2$) we can achieve up to 160 degrees of heating without the use of a hot chuck or oven. The question we asked was, is this sufficient, coupled with the acceleration achieved from increasing the current, to produce normal failures in a reasonable length of time, and in a way that could be used to predict lifetime under normal maximum operating conditions (1.6mA, 125°C junction temperature).

We have now characterized a large number of wafers using this test. Each coupon is mounted in a package and each device in the package is biased at a different level. We have chosen 14, 16, 18 and 20mA for the bias currents, with $V_{bc}=1$ and 2 at each bias current. 8-10 coupons were tested from each wafer. The advantage of mixing the devices in this manner is to sample each wafer site at each condition to avoid any systematic variation across the wafer.

One set of results is shown in figure 3. Assuming equation (1) applies to high currents then the slope of the curves is related to the value of n , the activation energy, and the junction temperature (which can be calculated). The ratio between values at the two V_{bc} values at a constant current can be used to calculate the activation energy directly from the junction temperature and measured lifetime values. It is then possible to calculate the MTTF at any junction current and temperature, as shown in figure 3. For this calculation we used $n=1$. Values of n derived from actual J-V data is generally close to 1, but show some variation from wafer to wafer, as generally a smaller number of samples is used, and the ratio between the currents is smaller making the calculation less accurate. Also shown in this plot are the values for MTTF at 125°C for this wafer determined from 3T measurements at 1.6mA, and a line showing the exponential fit to the medians of the data, which usually gives a good

approximation to the calculated MTTF. In this plot all the measured data points are shown. One major uncertainty in the technique as we have implemented it, is that the packages are un-cooled and the package temperature (and consequently the junction temperature) increase significantly. We estimate the chip backside temperature reaches at least 50°C in our present configuration.

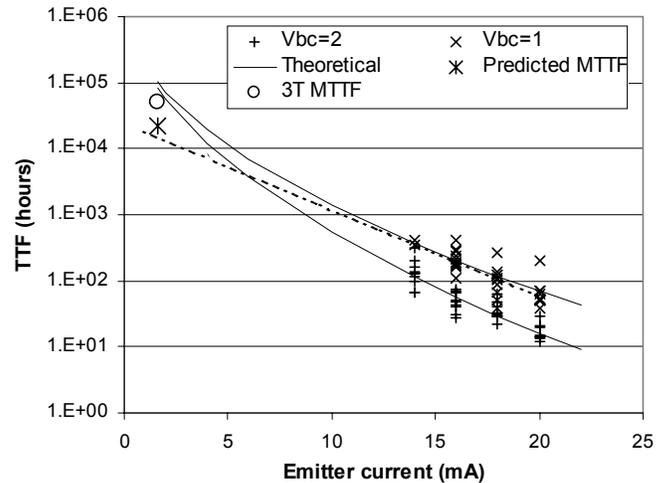


Figure 3. Comparison of J-T and 3T results.

CURRENT, VOLTAGE AND TEMPERATURE STRESS (J-V-T STRESS)

By increasing the ambient temperature we can further decrease the time to failure. We have chosen 125°C as the

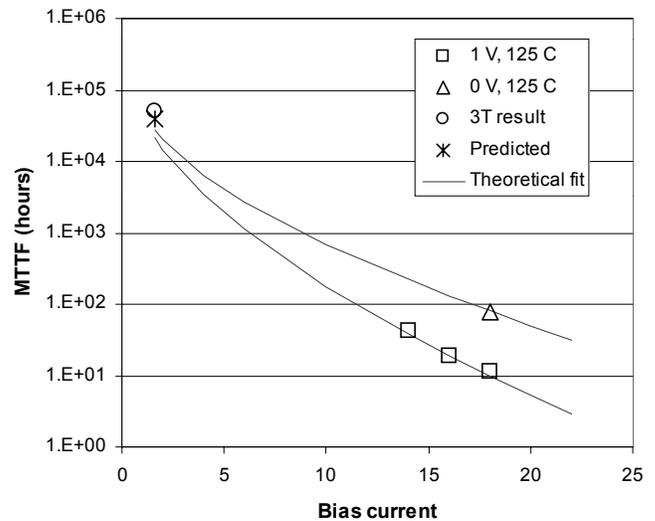


Figure 4. Comparison J-V-T and 3T results from the same wafer

ambient temperature. We have slightly modified the stress conditions to account for changes in the device performance at elevated temperatures, and to allow easy biasing in an oven environment. After some experimentation we have adopted emitter currents of 14, 16 and 18mA, with $V_{bc}=1$ and 0V, or with $V_{bc}=1$ and 2 volts for longer lifetime devices. Because of the improved equalization in the oven fixtures the potential temperature error in these tests is significantly less than in the J-V tests described above. J-V-T results for the same wafer used for the J-V test are compared with the 3T test results in figure 4. Only the median values are shown for clarity, and a value of $n=1$ was used. It is clearly demonstrated that excellent agreement between the two techniques can be achieved. It should be noted that these results were determined from devices on epitaxial material that gave poor reliability performance. Good agreement between results of the three techniques has also been obtained on more normal material with a higher MTTF.

BASE EMITTER DIODE STRESS (B-E STRESS)

Analysis of the Gummel plots of devices stressed to failure using each of the methods described so far show they are essentially identical, showing an increase in the ideality factor of the base current from 1.2 to 2. This implies that all the techniques cause the device to fail in the same way, by causing an increase in recombination either at the B-E junction or in the emitter shelf region. This suggests that identical failures could be created by biasing the base-emitter junction with the collector terminal floating. This is further supported by an observed correlation between the base current measured at normal bias, and fail time. Some advantages of this technique would be: the danger of oscillation is completely avoided, the coupons required for these tests can be significantly reduced in size (or made more compact) as no stabilization is required, and the number of electrical connections to each device is also reduced.

To investigate this further we have performed lifetime tests on devices as diodes. In figure 5 we compare the CFD results of B-E and J-V stress tests on the same wafer. A similar sigma is observed for both types of bias, and the Gummel plots of the failed devices are essentially identical. If we assume the lifetime is related to the recombination rate, (given by the base current), and that the level of recombination is the same under both bias conditions, then the ratio of the measured lifetimes at the same emitter current would be given by beta, as the junction temperature would be similar under each condition. Obviously the above assumptions grossly over-simplify the situation, however if we plot the product of MTTF and beta against bias current the results are in reasonably good agreement with the fail times for the same wafer under J-V stress, as shown in figure 6. Better agreement is, however, obtained using a simple exponential function instead of beta. The solid curve in the figure is given by:

$$MTTF = A \cdot \exp(Ea/kT) \cdot Je^{-n} \cdot \exp(-Ib/3.5) \quad (2)$$

Where I_b is the base current.

We are still awaiting results to determine if a similar expression describes the behavior of a longer-lived, more normal device. We are also evaluating this technique further to establish the optimum bias conditions, and evaluate the degree of correlation between B-E and 3T stress results. Of course this method cannot identify any issues associated with the collector region, or the base-collector junction (such as can occur in double hetero-junction devices).

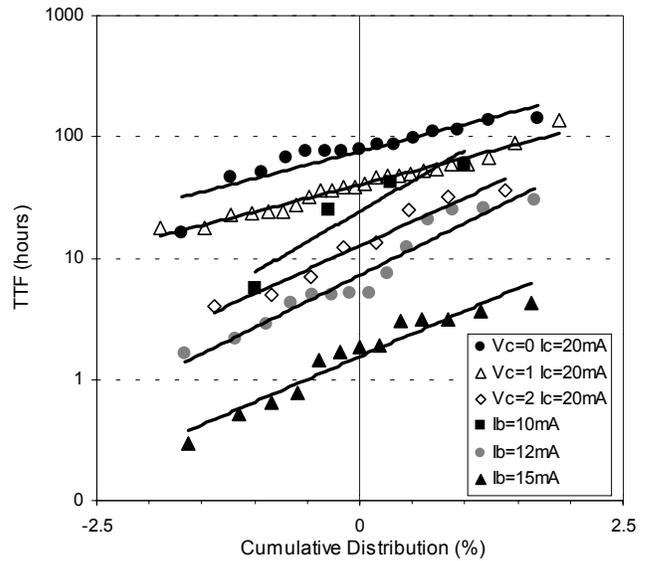


Figure 5. CFDs of B-E and J-V results from the same wafer.

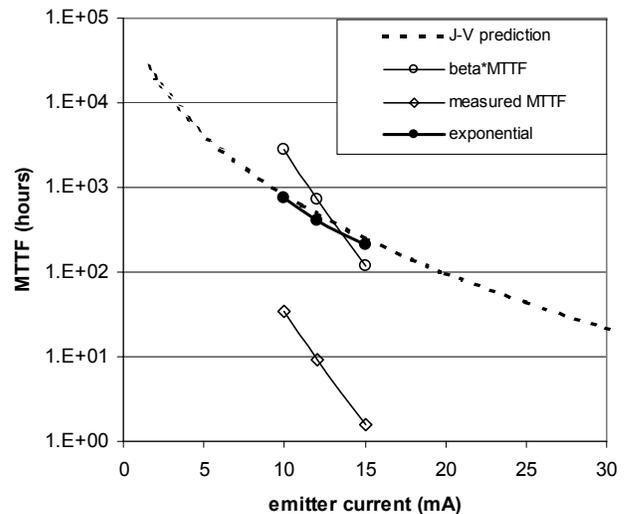


Figure 6. J-V and B-E test results for the same wafer.

CONCLUSIONS

We have shown that high bias currents can be used to accelerate the aging of HBTs. By stressing at current densities of over ten times the normal level we can achieve a similar or greater reduction in the length of reliability tests, without resorting to excessive overheating of the devices.

Testing devices at 12.5-15 times the maximum operating current has been used as the basis of a reliability screening technique that has been in use for many years. By monitoring the time to failure under different current and temperature (voltage) stress levels we can extrapolate to find the expected MTTF of devices under normal-maximum operating conditions. In general the agreement between 3T, J-V and J-V-T results is excellent. We have observed that the failure time is inversely proportional to emitter current once the temperature is normalized.

By biasing devices as base-emitter diodes very rapid estimation of reliability can be achieved, although this B-E stress technique needs further investigation to determine if it is generally applicable.

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ACRONYMS

CFD	Cumulative Failure Distribution
Ea	Activation Energy
ESD	Electro-Static Discharge.
FIT	Failures in Time. For telecommunications this is usually the number of failures in 10^9 hours of operation in 20 years of service.
HBT	Heterojunction Bipolar Transistor
MTTF	Median Time to Failure
TTF	Time to Failure